



H61H2-A

Rev : 1.0

ECS CONFIDENTIAL

TABLE OF CONTENTS

Page	Index
1	Cover Page
2	Block Diagram
3	CPU - DMI/FDI/PEG
4	CPU - MISC
5	CPU - DDR3
6	CPU - PWR/GND
7	DDR3 - CH_A_DIMM1
8	DDR3 - CH_B_DIMM3
9	VCORE / VAXG UP1625
10	VCORE / VAXG UP6281
11	DC/DC CPUVTT-UP1525 / VCCSA
12	DC/DC VDIMM / DDR_VTT/ 5VDUAL
13	Front Panel,FAN,PowerConn,GND,104
14	PCH - DMI/PCI/PE/USB
15	PCH - SATA / CLK
16	PCH - MISC, Strap Function
17	PCH - DP/VGA/FDI
18	PCH - PWR
19	PCH - GND
20	Slot - PCI-EX16/PCI-EX1
21	DVI CONN&COM&PS2
22	USB/SATA/SPI
23	SIO-IT8728 CX
24	AUDIO VT1705/ALC662(CHIP)
25	AUDIO VT1705/ALC662(PANEL)

Page	Index
26	IT8893(PCIE TO PCI)
27	Slot - PCI1&PCI2
28	PCIE LAN RTL8111E/8105E
29	Power Delivery
30	Power Sequence, Reset Diagram
31	Clock Distribution

REVISION HISTORY:

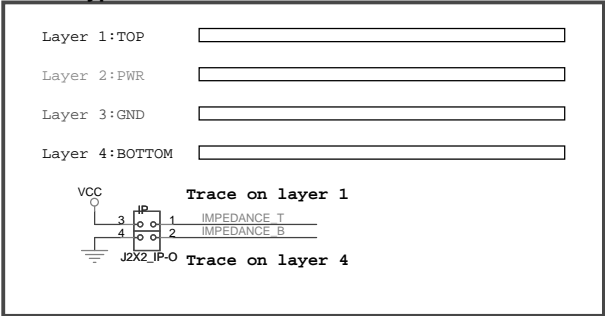
Rev	Date	Notes
V.A	2010/12/16	Change from H67H2-M3: 1. Rear IO(VGA and DVI) 2. Three PCIEX1 Slots 3. Super IO change to IT8728 4. CPU PWM and VCCIO change to UPI 5. Remove USB3.0 6. Remove EZ Charger
V.1.0	2011/01/20 81-605-Y96100	Change from V.A: 1.All-Solid Capacitor 2.Fix EZ charger 3. RT to 0402

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RD - ELI
LAYOUT : Bing

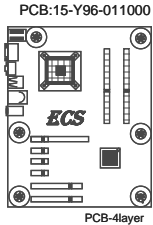
NOTE:
Design by 428971_428971_Sugar_Bay_and_BromolowWS_PDG_Rev1_5.pdf
443554_443554_Intel6Series_C200Series_Chipset_EDS_Rev1_5.pdf

Circuit type 1



PCB Impedance control

Impedance (OHM)	Trace Width (mil)	Trace Width (S/W/S)	Trace Length (inch)	Pre-preg	Default
50	4	(16/4/16)	8	1080	TOP BOTTOM
60	5	(20/5/20)	10	2116	INT



PCB STACK:
L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

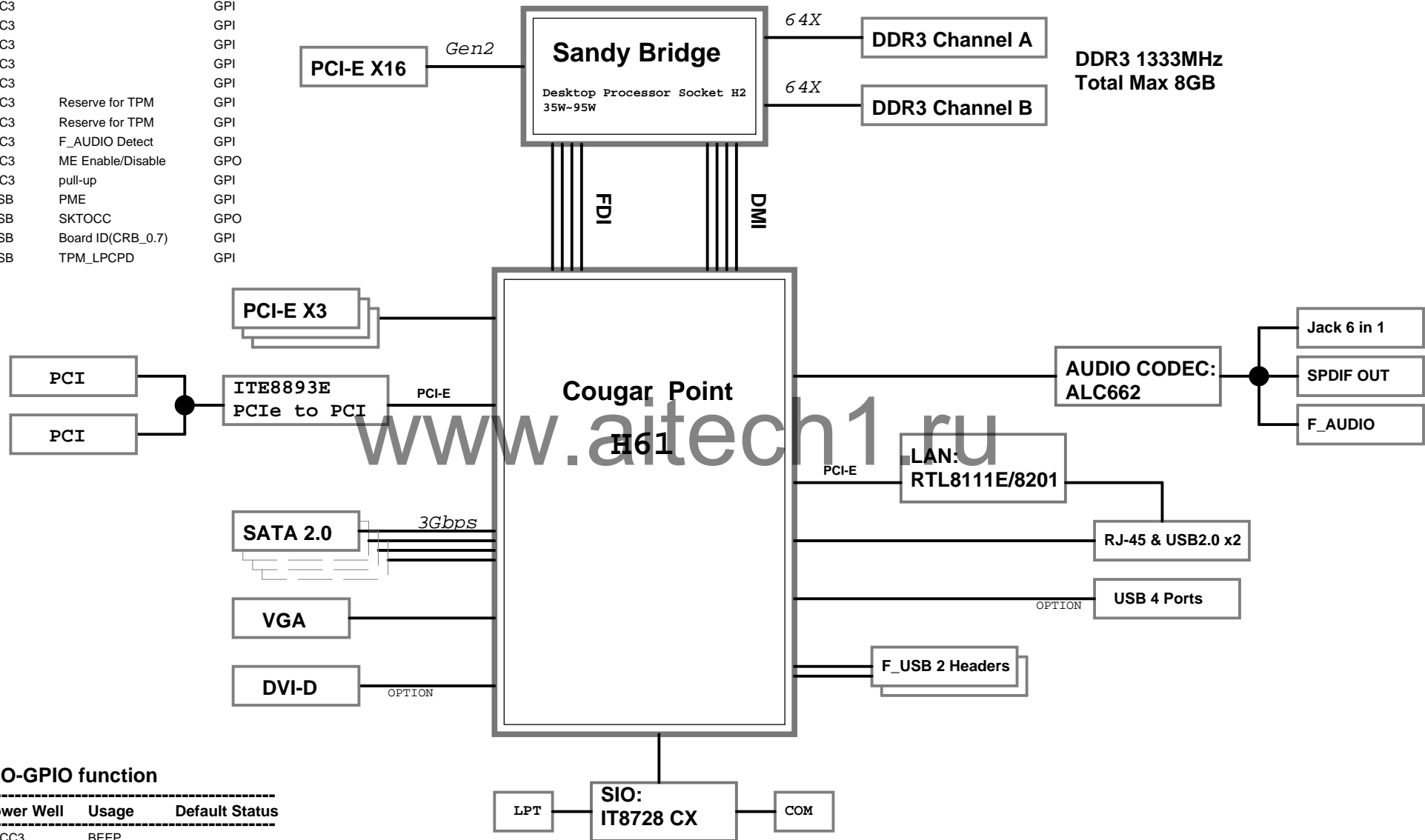


Elitegroup Computer Systems

Title	Cover Page	Rev	1.0
Size	Document Number	H61H2-A	
Date:	Thursday, January 27, 2011	Sheet	1 of 31

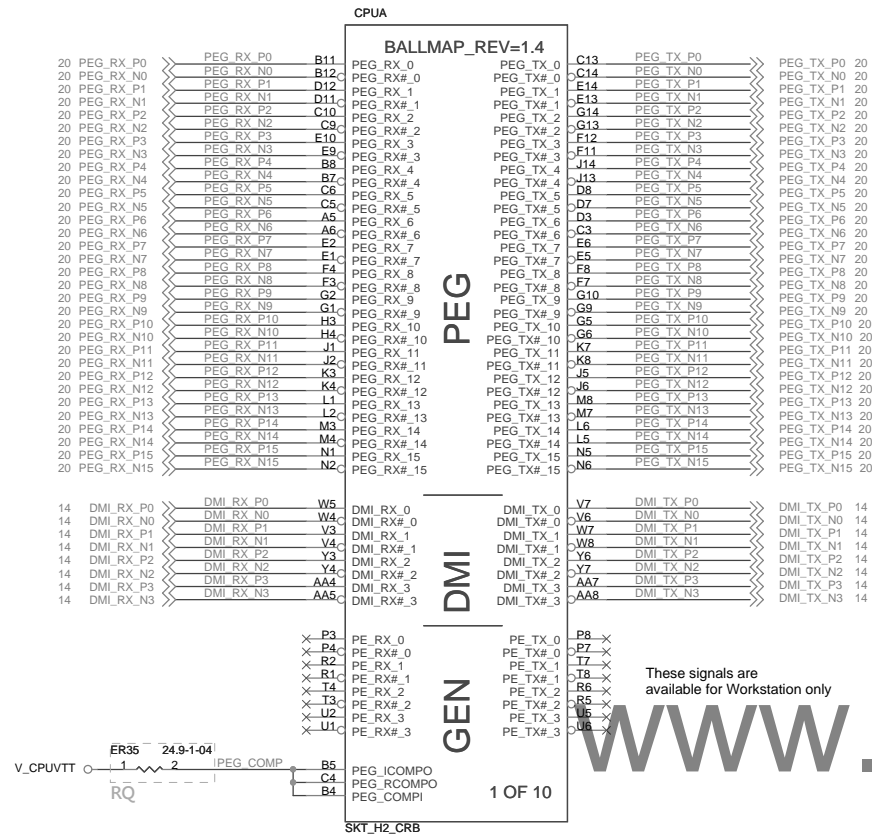
PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3		GPI
GPIO22	VCC3		GPI
GPIO38	VCC3		GPI
GPIO39	VCC3		GPI
GPIO48	VCC3		GPI
GPIO21	VCC3		GPI
GPIO36	VCC3		GPI
GPIO37	VCC3		GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO0	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI



SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16	VCC3	BEEP	
GP23		Power LED	
GP22		Power LED	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	



These signals are available for Workstation only

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SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4MIL TRACE TO RQ.
1 ROUTE B5 TO RQ. 1 AS A SEPERATE 12MIL TRACE.

01-201-082010 PCH BD82H61 B2

11-018-115124 SOCKET.CPU.LGA 1155P SMD.G/F.BLACK.ACA-ZIF-096-P02.LOTES

11-018-115013 SOCKET.CPU.LGA 1155P SMD.G/F.BLACK.2069965-3.TYCO

20-800-005111 SUBASSY.STEEL.LGA 1155P.W/BACK PLATE.ACA-ZIF-082-P23.LOTES

20-800-004811 SUBASSY.STEEL.LGA 1156P.W/BACK PLATE.2069838-4.TYCO



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Title		CPU - DMI/FDI/PEG	
Size	Document Number	H61H2-A	
Custom		Rev 1.0	
Date:	Wednesday, January 26, 2011	Sheet	3 of 31

CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

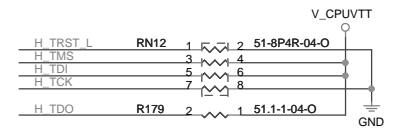
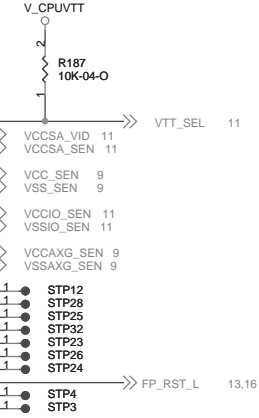
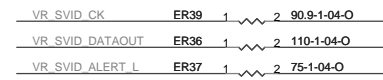
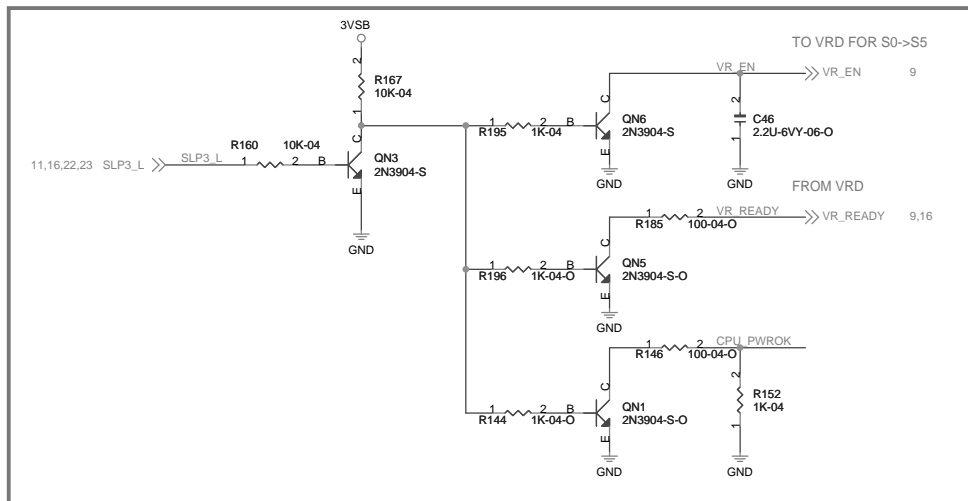
CFG[0..17] HAVE INTERNAL PULL-UPS

PCIE CONFIG	SEL0	SEL1
1 X 16	1	1
2 X 8	0	1

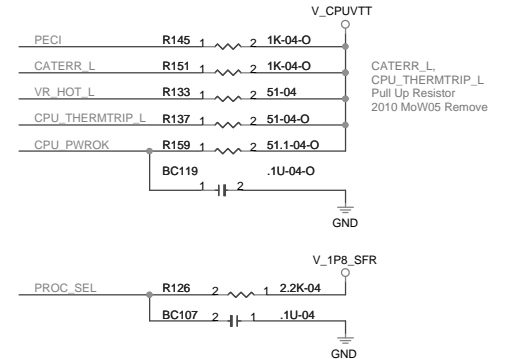
CFG[5:6]:
 01=DEFAULT X16,
 01=2X8,
 10=RESERVED,
 00=X8,X4,X4

change test point for internal PU Jack05/25

Power Down Sequencing Circuit



EDS P68/132 has internal PU Jack05/25



DMI/FDI termination voltage:
 DC coupled: TX/RX to VCC ISF sampled high
 DC coupled: TX/RX TO VSS IF sampled low
 AC COUPLED: TX set to VCC/2, RX set to VSS regardless of this strap

7 M_DATA_A[0..63]	<<>	M_DATA A[0..63]
7 M_DQS_A_P[0..7]	<<>	M DQS A P[0..7]
7 M_DQS_A_N[0..7]	<<>	M DQS A N[0..7]
7 M_MA_A[0..15]	<<>	M MA A[0..15]
7 M_BS_A[0..2]	<<>	M BS A[0..2]
7 M_CS_A_L[0..1]	<<>	M CS A L[0..1]
7 M_CKE_A[0..1]	<<>	M CKE A[0..1]
7 M_ODT_A[0..1]	<<>	M ODT A[0..1]
7 M_CLK_A_P[0..1]	<<>	M CLK A P[0..1]
7 M_CLK_A_N[0..1]	<<>	M CLK A N[0..1]
7 M_WE_A_L	<<>	M WE A L
7 M_CAS_A_L	<<>	M CAS A L
7 M_RAS_A_L	<<>	M RAS A L

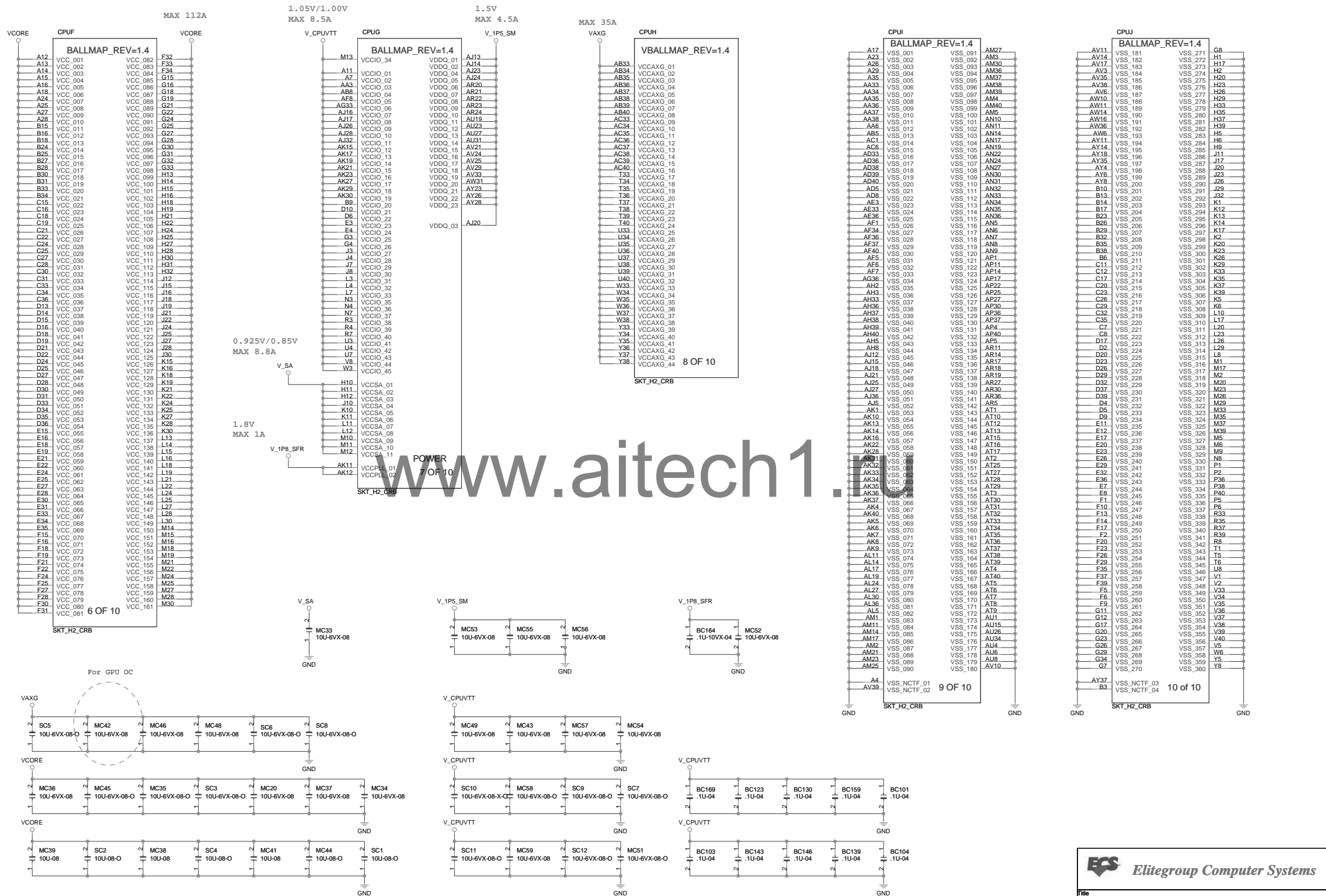
DDR3 CH.A

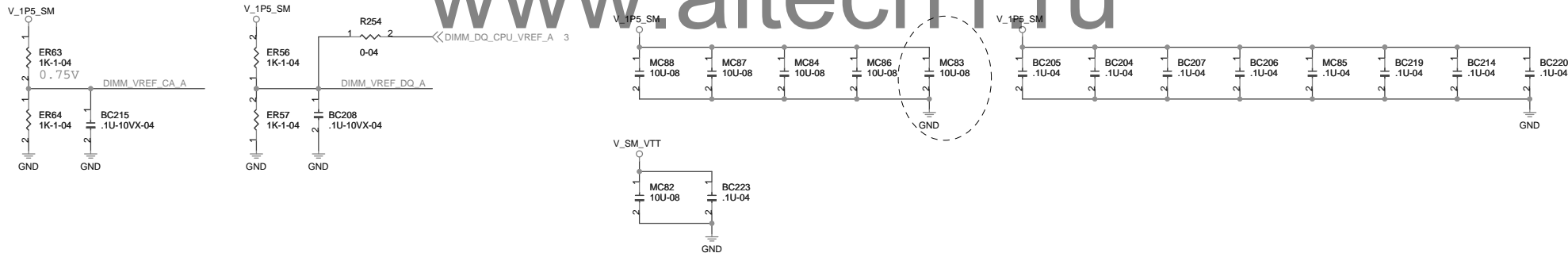
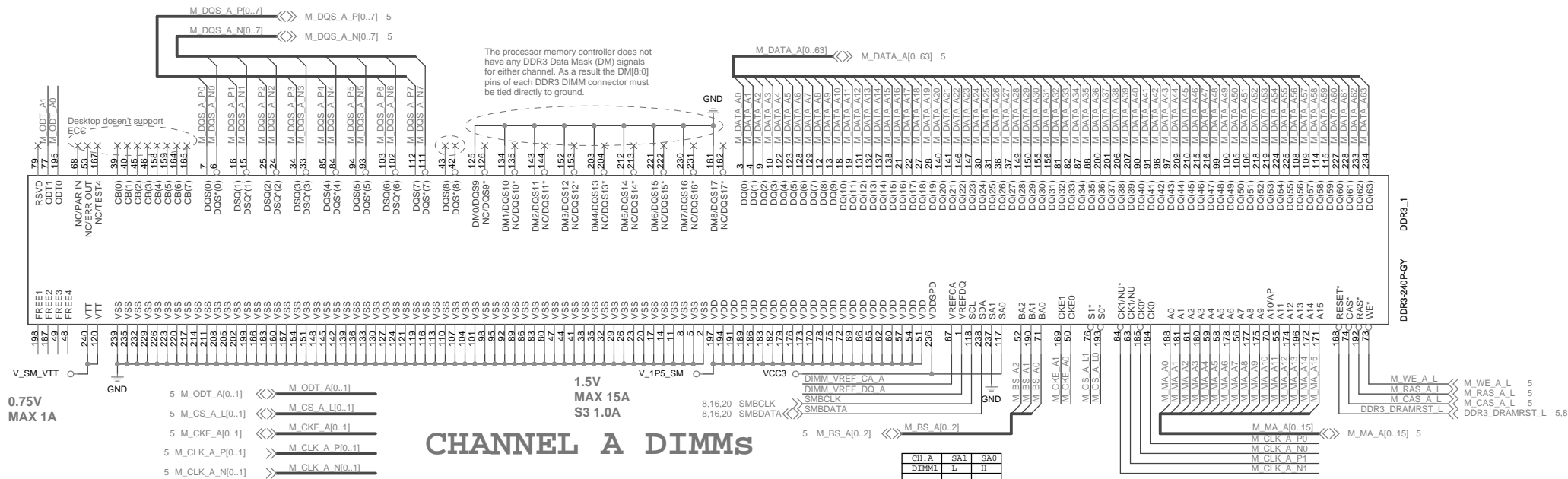
7,8 DDR3_DRAMRST_L <<> DDR3_DRAMRST_L

8 M_DATA_B[0..63]	<<>	M_DATA B[0..63]
8 M_DQS_B_P[0..7]	<<>	M DQS B P[0..7]
8 M_DQS_B_N[0..7]	<<>	M DQS B N[0..7]
8 M_MA_B[0..15]	<<>	M MA B[0..15]
8 M_BS_B[0..2]	<<>	M BS B[0..2]
8 M_CS_B_L[0..1]	<<>	M CS B L[0..1]
8 M_CKE_B[0..1]	<<>	M CKE B[0..1]
8 M_ODT_B[0..1]	<<>	M ODT B[0..1]
8 M_CLK_B_P[0..1]	<<>	M CLK B P[0..1]
8 M_CLK_B_N[0..1]	<<>	M CLK B N[0..1]
8 M_WE_B_L	<<>	M WE B L
8 M_CAS_B_L	<<>	M CAS B L
8 M_RAS_B_L	<<>	M RAS B L

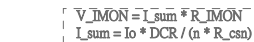
DDR3 CH.B

CPUC		BALLMAP_REV=1.4	
M_DATA_A0	AJ3	SA_DQ_0	SA_MA_0
M_DATA_A1	AJ4	SA_DQ_1	SA_MA_1
M_DATA_A2	AL3	SA_DQ_2	SA_MA_2
M_DATA_A3	AL4	SA_DQ_3	SA_MA_3
M_DATA_A4	AJ2	SA_DQ_4	SA_MA_4
M_DATA_A5	AJ1	SA_DQ_5	SA_MA_5
M_DATA_A6	AL2	SA_DQ_6	SA_MA_6
M_DATA_A7	AL1	SA_DQ_7	SA_MA_7
M_DATA_A8	AN1	SA_DQ_8	SA_MA_8
M_DATA_A9	AR3	SA_DQ_9	SA_MA_9
M_DATA_A10	AR4	SA_DQ_10	SA_MA_10
M_DATA_A11	AN2	SA_DQ_11	SA_MA_11
M_DATA_A12	AN3	SA_DQ_12	SA_MA_12
M_DATA_A13	AR2	SA_DQ_13	SA_MA_13
M_DATA_A14	AR1	SA_DQ_14	SA_MA_14
M_DATA_A15	AV2	SA_DQ_15	SA_MA_15
M_DATA_A16	AV3	SA_DQ_16	SA_MA_16
M_DATA_A17	AV4	SA_DQ_17	SA_MA_17
M_DATA_A18	AV5	SA_DQ_18	SA_MA_18
M_DATA_A19	AU2	SA_DQ_19	SA_MA_19
M_DATA_A20	AU3	SA_DQ_20	SA_MA_20
M_DATA_A21	AU4	SA_DQ_21	SA_MA_21
M_DATA_A22	AU5	SA_DQ_22	SA_MA_22
M_DATA_A23	AY5	SA_DQ_23	SA_MA_23
M_DATA_A24	AY7	SA_DQ_24	SA_MA_24
M_DATA_A25	AU7	SA_DQ_25	SA_MA_25
M_DATA_A26	AV9	SA_DQ_26	SA_MA_26
M_DATA_A27	AV8	SA_DQ_27	SA_MA_27
M_DATA_A28	AV7	SA_DQ_28	SA_MA_28
M_DATA_A29	AW7	SA_DQ_29	SA_MA_29
M_DATA_A30	AW9	SA_DQ_30	SA_MA_30
M_DATA_A31	AY9	SA_DQ_31	SA_MA_31
M_DATA_A32	AU35	SA_DQ_32	SA_MA_32
M_DATA_A33	AW37	SA_DQ_33	SA_MA_33
M_DATA_A34	AU39	SA_DQ_34	SA_MA_34
M_DATA_A35	AU36	SA_DQ_35	SA_MA_35
M_DATA_A36	AW35	SA_DQ_36	SA_MA_36
M_DATA_A37	AY38	SA_DQ_37	SA_MA_37
M_DATA_A38	AU38	SA_DQ_38	SA_MA_38
M_DATA_A39	AU37	SA_DQ_39	SA_MA_39
M_DATA_A40	AR40	SA_DQ_40	SA_MA_40
M_DATA_A41	AR37	SA_DQ_41	SA_MA_41
M_DATA_A42	AN37	SA_DQ_42	SA_MA_42
M_DATA_A43	AR39	SA_DQ_43	SA_MA_43
M_DATA_A44	AR38	SA_DQ_44	SA_MA_44
M_DATA_A45	AN38	SA_DQ_45	SA_MA_45
M_DATA_A46	AN39	SA_DQ_46	SA_MA_46
M_DATA_A47	AN40	SA_DQ_47	SA_MA_47
M_DATA_A48	AL48	SA_DQ_48	SA_MA_48
M_DATA_A49	AJ37	SA_DQ_49	SA_MA_49
M_DATA_A50	AJ38	SA_DQ_50	SA_MA_50
M_DATA_A51	AJ37	SA_DQ_51	SA_MA_51
M_DATA_A52	AL39	SA_DQ_52	SA_MA_52
M_DATA_A53	AL38	SA_DQ_53	SA_MA_53
M_DATA_A54	AJ39	SA_DQ_54	SA_MA_54
M_DATA_A55	AJ40	SA_DQ_55	SA_MA_55
M_DATA_A56	AG40	SA_DQ_56	SA_MA_56
M_DATA_A57	AG37	SA_DQ_57	SA_MA_57
M_DATA_A58	AE38	SA_DQ_58	SA_MA_58
M_DATA_A59	AE37	SA_DQ_59	SA_MA_59
M_DATA_A60	AG38	SA_DQ_60	SA_MA_60
M_DATA_A61	AE39	SA_DQ_61	SA_MA_61
M_DATA_A62	AE38	SA_DQ_62	SA_MA_62
M_DATA_A63	AE40	SA_DQ_63	SA_MA_63
M_DQS_A_P0	AK3	SA_DQS_0	SA_MA_64
M_DQS_A_P1	AP3	SA_DQS_1	SA_MA_65
M_DQS_A_P2	AW4	SA_DQS_2	SA_MA_66
M_DQS_A_P3	AV8	SA_DQS_3	SA_MA_67
M_DQS_A_P4	AV37	SA_DQS_4	SA_MA_68
M_DQS_A_P5	AP38	SA_DQS_5	SA_MA_69
M_DQS_A_P6	AK38	SA_DQS_6	SA_MA_70
M_DQS_A_P7	AF38	SA_DQS_7	SA_MA_71
M_DQS_A_N0	AK2	SA_DQS#_0	SA_MA_72
M_DQS_A_N1	AP2	SA_DQS#_1	SA_MA_73
M_DQS_A_N2	AV4	SA_DQS#_2	SA_MA_74
M_DQS_A_N3	AW8	SA_DQS#_3	SA_MA_75
M_DQS_A_N4	AV36	SA_DQS#_4	SA_MA_76
M_DQS_A_N5	AP39	SA_DQS#_5	SA_MA_77
M_DQS_A_N6	AK39	SA_DQS#_6	SA_MA_78
M_DQS_A_N7	AF39	SA_DQS#_7	SA_MA_79
SA_WE#		SA_MA_80	SA_MA_80
SA_CAS#		SA_MA_81	SA_MA_81
SA_RAS#		SA_MA_82	SA_MA_82
SA_BS_0		SA_MA_83	SA_MA_83
SA_BS_1		SA_MA_84	SA_MA_84
SA_BS_2		SA_MA_85	SA_MA_85
SA_CS#_0		SA_MA_86	SA_MA_86
SA_CS#_1		SA_MA_87	SA_MA_87
SA_CS#_2		SA_MA_88	SA_MA_88
SA_CS#_3		SA_MA_89	SA_MA_89
SA_CKE_0		SA_MA_90	SA_MA_90
SA_CKE_1		SA_MA_91	SA_MA_91
SA_CKE_2		SA_MA_92	SA_MA_92
SA_CKE_3		SA_MA_93	SA_MA_93
SA_ODT_0		SA_MA_94	SA_MA_94
SA_ODT_1		SA_MA_95	SA_MA_95
SA_ODT_2		SA_MA_96	SA_MA_96
SA_ODT_3		SA_MA_97	SA_MA_97
SA_ECC_CB_0		SA_MA_98	SA_MA_98
SA_ECC_CB_1		SA_MA_99	SA_MA_99
SA_ECC_CB_2		SA_MA_100	SA_MA_100
SA_ECC_CB_3		SA_MA_101	SA_MA_101
SA_ECC_CB_4		SA_MA_102	SA_MA_102
SA_ECC_CB_5		SA_MA_103	SA_MA_103
SA_ECC_CB_6		SA_MA_104	SA_MA_104
SA_ECC_CB_7		SA_MA_105	SA_MA_105
SM_DRAMRST#		SA_MA_106	SA_MA_106
SA_DQS_8		SA_MA_107	SA_MA_107
SA_DQS#_8		SA_MA_108	SA_MA_108
SA_ECC_CB_8		SA_MA_109	SA_MA_109
SA_ECC_CB_9		SA_MA_110	SA_MA_110
SA_ECC_CB_10		SA_MA_111	SA_MA_111
SA_ECC_CB_11		SA_MA_112	SA_MA_112
SA_ECC_CB_12		SA_MA_113	SA_MA_113
SA_ECC_CB_13		SA_MA_114	SA_MA_114
SA_ECC_CB_14		SA_MA_115	SA_MA_115
SA_ECC_CB_15		SA_MA_116	SA_MA_116
SA_ECC_CB_16		SA_MA_117	SA_MA_117
SA_ECC_CB_17		SA_MA_118	SA_MA_118
SA_ECC_CB_18		SA_MA_119	SA_MA_119
SA_ECC_CB_19		SA_MA_120	SA_MA_120
SA_ECC_CB_20		SA_MA_121	SA_MA_121
SA_ECC_CB_21		SA_MA_122	SA_MA_122
SA_ECC_CB_22		SA_MA_123	SA_MA_123
SA_ECC_CB_23		SA_MA_124	SA_MA_124
SA_ECC_CB_24		SA_MA_125	SA_MA_125
SA_ECC_CB_25		SA_MA_126	SA_MA_126
SA_ECC_CB_26		SA_MA_127	SA_MA_127
SA_ECC_CB_27		SA_MA_128	SA_MA_128
SA_ECC_CB_28		SA_MA_129	SA_MA_129
SA_ECC_CB_29		SA_MA_130	SA_MA_130
SA_ECC_CB_30		SA_MA_131	SA_MA_131
SA_ECC_CB_31		SA_MA_132	SA_MA_132
SA_ECC_CB_32		SA_MA_133	SA_MA_133
SA_ECC_CB_33		SA_MA_134	SA_MA_134
SA_ECC_CB_34		SA_MA_135	SA_MA_135
SA_ECC_CB_35		SA_MA_136	SA_MA_136
SA_ECC_CB_36		SA_MA_137	SA_MA_137
SA_ECC_CB_37		SA_MA_138	SA_MA_138
SA_ECC_CB_38		SA_MA_139	SA_MA_139
SA_ECC_CB_39		SA_MA_140	SA_MA_140
SA_ECC_CB_40		SA_MA_141	SA_MA_141
SA_ECC_CB_41		SA_MA_142	SA_MA_142
SA_ECC_CB_42		SA_MA_143	SA_MA_143
SA_ECC_CB_43		SA_MA_144	SA_MA_144
SA_ECC_CB_44		SA_MA_145	SA_MA_145
SA_ECC_CB_45		SA_MA_146	SA_MA_146
SA_ECC_CB_46		SA_MA_147	SA_MA_147
SA_ECC_CB_47		SA_MA_148	SA_MA_148
SA_ECC_CB_48		SA_MA_149	SA_MA_149
SA_ECC_CB_49		SA_MA_150	SA_MA_150
SA_ECC_CB_50		SA_MA_151	SA_MA_151
SA_ECC_CB_51		SA_MA_152	SA_MA_152
SA_ECC_CB_52		SA_MA_153	SA_MA_153
SA_ECC_CB_53		SA_MA_154	SA_MA_154
SA_ECC_CB_54		SA_MA_155	SA_MA_155
SA_ECC_CB_55		SA_MA_156	SA_MA_156
SA_ECC_CB_56		SA_MA_157	SA_MA_157
SA_ECC_CB_57		SA_MA_158	SA_MA_158
SA_ECC_CB_58		SA_MA_159	SA_MA_159
SA_ECC_CB_59		SA_MA_160	SA_MA_160
SA_ECC_CB_60		SA_MA_161	SA_MA_161
SA_ECC_CB_61		SA_MA_162	SA_MA_162
SA_ECC_CB_62		SA_MA_163	SA_MA_163
SA_ECC_CB_63		SA_MA_164	SA_MA_164
SA_ECC_CB_64		SA_MA_165	SA_MA_165
SA_ECC_CB_65		SA_MA_166	SA_MA_166
SA_ECC_CB_66		SA_MA_167	SA_MA_167
SA_ECC_CB_67		SA_MA_168	SA_MA_168
SA_ECC_CB_68		SA_MA_169	SA_MA_169
SA_ECC_CB_69		SA_MA_170	SA_MA_170
SA_ECC_CB_70		SA_MA_171	SA_MA_171
SA_ECC_CB_71		SA_MA_172	SA_MA_172
SA_ECC_CB_72		SA_MA_173	SA_MA_173
SA_ECC_CB_73		SA_MA_174	SA_MA_174
SA_ECC_CB_74		SA_MA_175	SA_MA_175
SA_ECC_CB_75		SA_MA_176	SA_MA_176
SA_ECC_CB_76		SA_MA_177	SA_MA_177
SA_ECC_CB_77		SA_MA_178	SA_MA_178
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SA_ECC_CB_79		SA_MA_180	SA_MA_180
SA_ECC_CB_80		SA_MA_181	SA_MA_181
SA_ECC_CB_81		SA_MA_182	SA_MA_182
SA_ECC_CB_82		SA_MA_183	SA_MA_183
SA_ECC_CB_83		SA_MA_184	SA_MA_184
SA_ECC_CB_84		SA_MA_185	SA_MA_185
SA_ECC_CB_85		SA_MA_186	SA_MA_186
SA_ECC_CB_86		SA_MA_187	SA_MA_187
SA_ECC_CB_87		SA_MA_188	SA_MA_188
SA_ECC_CB_88		SA_MA_189	SA_MA_189
SA_ECC_CB_89		SA_MA_190	SA_MA_190
SA_ECC_CB_90		SA_MA_191	SA_MA_191
SA_ECC_CB_91		SA_MA_192	SA_MA_192
SA_ECC_CB_92		SA_MA_193	SA_MA_193
SA_ECC_CB_93		SA_MA_194	SA_MA_194
SA_ECC_CB_94		SA_MA_195	SA_MA_195
SA_ECC_CB_95		SA_MA_196	SA_MA_196
SA_ECC_CB_96		SA_MA_197	SA_MA_197
SA_ECC_CB_97		SA_MA_198	SA_MA_198
SA_ECC_CB_98		SA_MA_199	SA_MA_199
SA_ECC_CB_99		SA_MA_200	SA_MA_200
SA_ECC_CB_100		SA_MA_201	SA_MA_201
SA_ECC_CB_101		SA_MA_202	SA_MA_202
SA_ECC_CB_102		SA_MA_203	SA_MA_203
SA_ECC_CB_103		SA_MA_204	SA_MA_204
SA_ECC_CB_104		SA_MA_205	SA_MA_205
SA_ECC_CB_105		SA_MA_206	SA_MA_206
SA_ECC_CB_106		SA_MA_207	SA_MA_207
SA_ECC_CB_107		SA_MA_208	SA_MA_208
SA_ECC_CB_108		SA_MA_209	SA_MA_209
SA_ECC_CB_109		SA_MA_210	SA_MA_210
SA_ECC_CB_110		SA_MA_211	SA_MA_211
SA_ECC_CB_111		SA_MA_212	SA_MA_212
SA_ECC_CB_112		SA_MA_213	SA_MA_213
SA_ECC_CB_113		SA_MA_214	SA_MA_214
SA_ECC_CB_114		SA_MA_215	SA_MA_215
SA_ECC_CB_115		SA_MA_216	SA_MA_216
SA_ECC_CB_116		SA_MA_217	SA_MA_217
SA_ECC_CB_117		SA_MA_218	SA_MA_218
SA_ECC_CB_118		SA_MA_219	SA_MA_219
SA_ECC_CB_119		SA_MA_220	SA_MA_220
SA_ECC_CB_120		SA_MA_221	SA_MA_221
SA_ECC_CB_121		SA_MA_222	SA_MA_222
SA_ECC_CB_122		SA_MA_223	SA_MA_223
SA_ECC_CB_123		SA_MA_224	SA_MA_224
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SA_ECC_CB_125		SA_MA_226	SA_MA_226
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SA_ECC_CB_127		SA_MA_228	SA_MA_228
SA_ECC_CB_128		SA_MA_229	SA_MA_229
SA_ECC_CB_129		SA_MA_230	SA_MA_230
SA_ECC_CB_130		SA_MA_231	SA_MA_231
SA_ECC_CB_131		SA_MA_232	SA_MA_232
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SA_ECC_CB_133		SA_MA_234	SA_MA_234
SA_ECC_CB_134		SA_MA_235	SA_MA_235
SA_ECC_CB_135		SA_MA_236	SA_MA_236
SA_ECC_CB_136		SA_MA_237	SA_MA_237
SA_ECC_CB_137		SA_MA_238	SA_MA_238
SA_ECC_CB_138		SA_MA_239	SA_MA_239
SA_ECC_CB_139		SA_MA_240	SA_MA_240
SA_ECC_CB_140		SA_MA_241	SA_MA_241
SA_ECC_CB_141		SA_MA_242	SA_MA_242
SA_ECC_CB_142		SA_MA_243	SA_MA_243
SA_ECC_CB_143		SA_MA_244	SA_MA_244
SA_ECC_CB_144		SA_MA_245	SA_MA_245
SA_ECC_CB_145		SA_MA_246	SA_MA_246
SA_ECC_CB_146		SA_MA_247	SA_MA_247
SA_ECC_CB_147		SA_MA_248	SA_MA_248
SA_ECC_CB_148		SA_MA_249	SA_MA_249
SA_ECC_CB_149		SA_MA_250	SA_MA_250
SA_ECC_CB_150		SA_MA_251	SA_MA_251
SA_ECC_CB_151		SA_MA_252	SA_MA_252



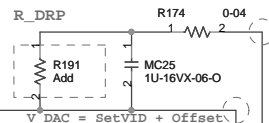


VCC	O	—	OVCC
VCORE	O	—	OVCORE
V_CPUVTT	O	—	OV_CPUVTT
+12V_4P	O	—	O+12V_4P
VCC3	O	—	OVCC3
VIN	O	—	OVIN
VAXG	O	—	OVAXG
5VSB	O	—	O5VSB



Css close to DAC

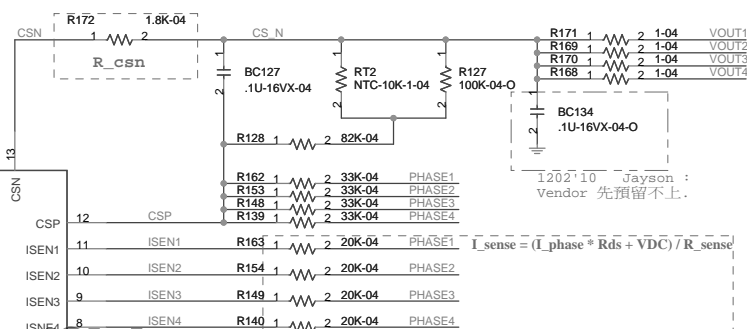
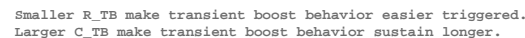
```
R_DRP      R174      0-04      V_EAP = V_DAC - I_sum * D_DRP
```


$$tVID + Offsetv$$
$$\begin{aligned} \overline{V_{IMON}} &= \overline{I_{sum}} * \overline{R_{IMON}} \\ I_{sum} &= I_o * DCR / (n * R_{csn}) \end{aligned}$$

Phase Frequency :

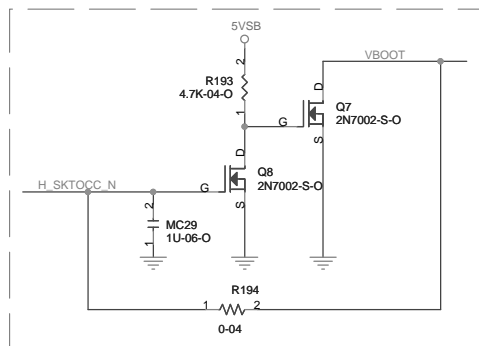
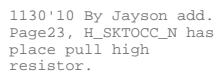
$$f_{sw} = 300 * (27k / RT)^{0.83}$$

$$RT = 25k \rightarrow f_{sw} = 300k \text{ Hz}$$



1202'10 Jayson :
Vendor 先預留不上

$$\overline{I_{\text{sense}}} = (\overline{I_{\text{phase}}} * \overline{R_{\text{ds}}} + \overline{V_{\text{DC}}}) / \overline{R_{\text{sense}}}$$



```
VBOOT :
VCC -> VCORE / VAXG boot 1.1V
GND -> VCORE / VAXG boot 0V
```

```

POR condition : VCC5 > 4.3V AND VCC12 > 9.5V AND ENPWR > 0.65V
OCP condition : V_IMON > 1.3 * V_IMAX for total current
                  I_CSNx > 100uA for channel current
OVP condition : V_FB - V_EAP > 150mV
UVP condition : V_FB < 200mV

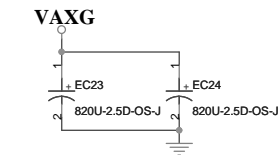
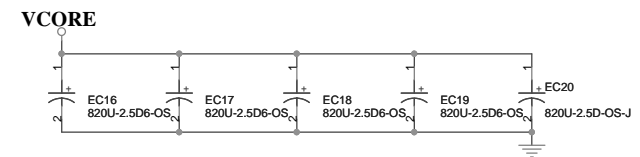
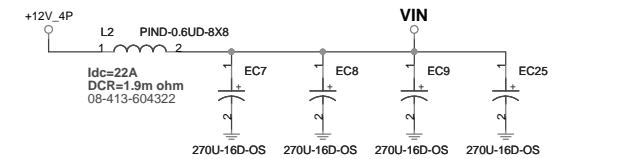
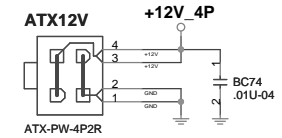
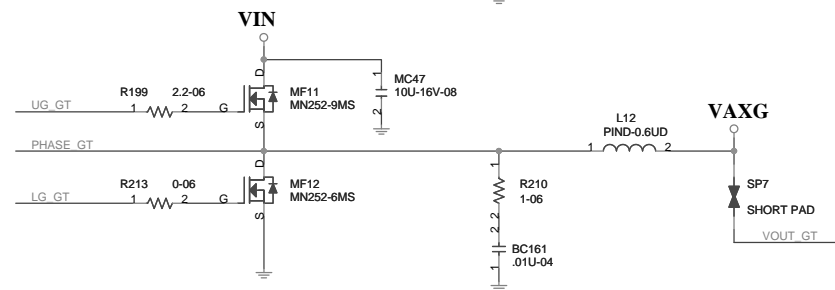
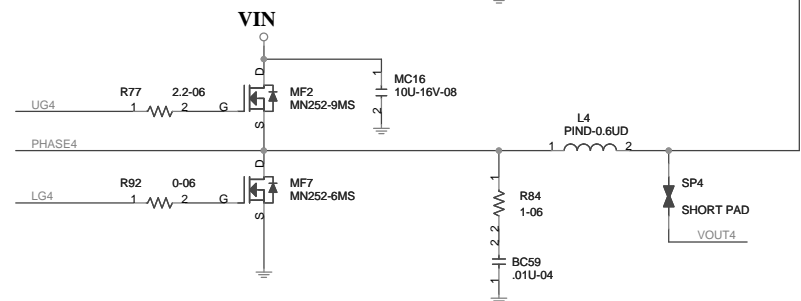
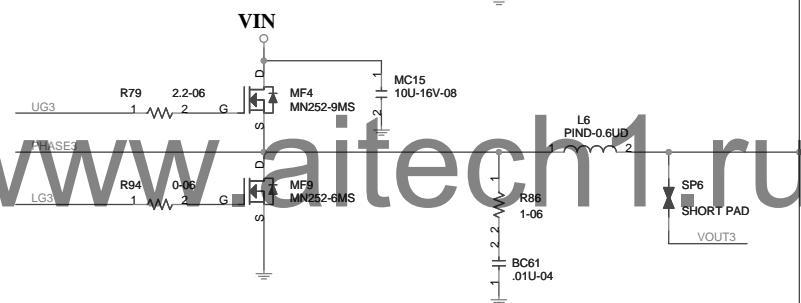
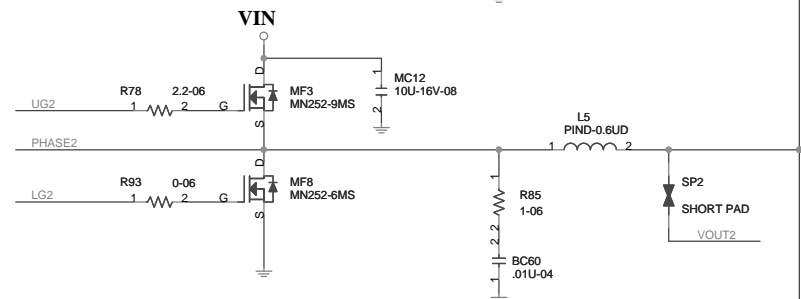
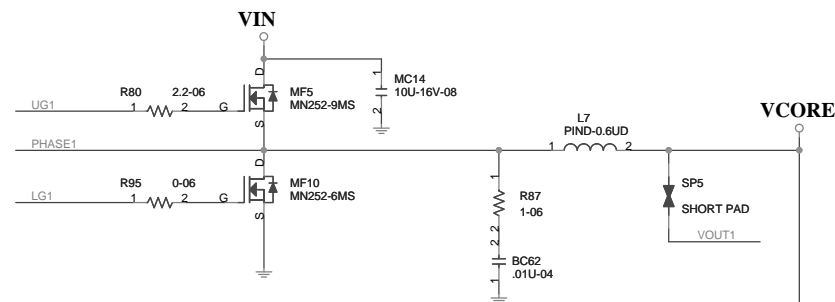
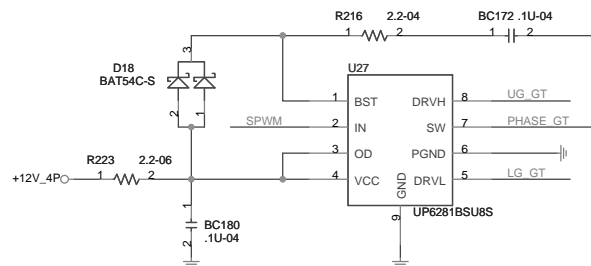
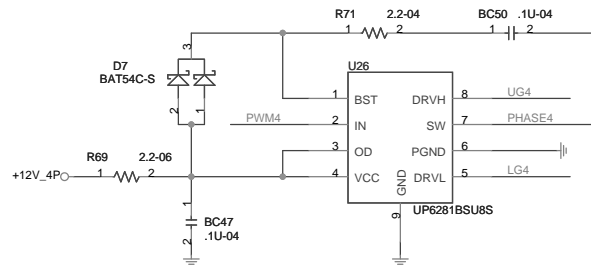
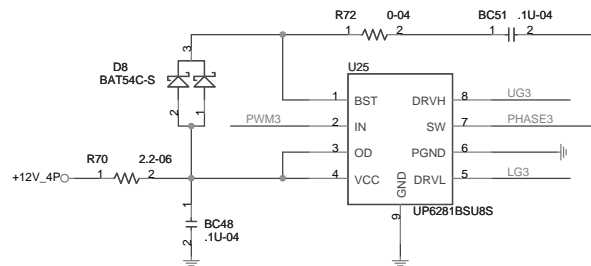
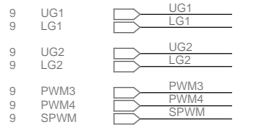
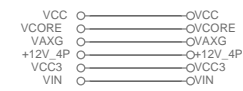
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Elitegroup Computer Systems

Title			
VCORE / VAXG UP1625			
Size	Document Number	Rev	
Custom	H61H2-A	1.0	
Date:	Thursday, January 27, 2011	Sheet	9 of 31

External Connection

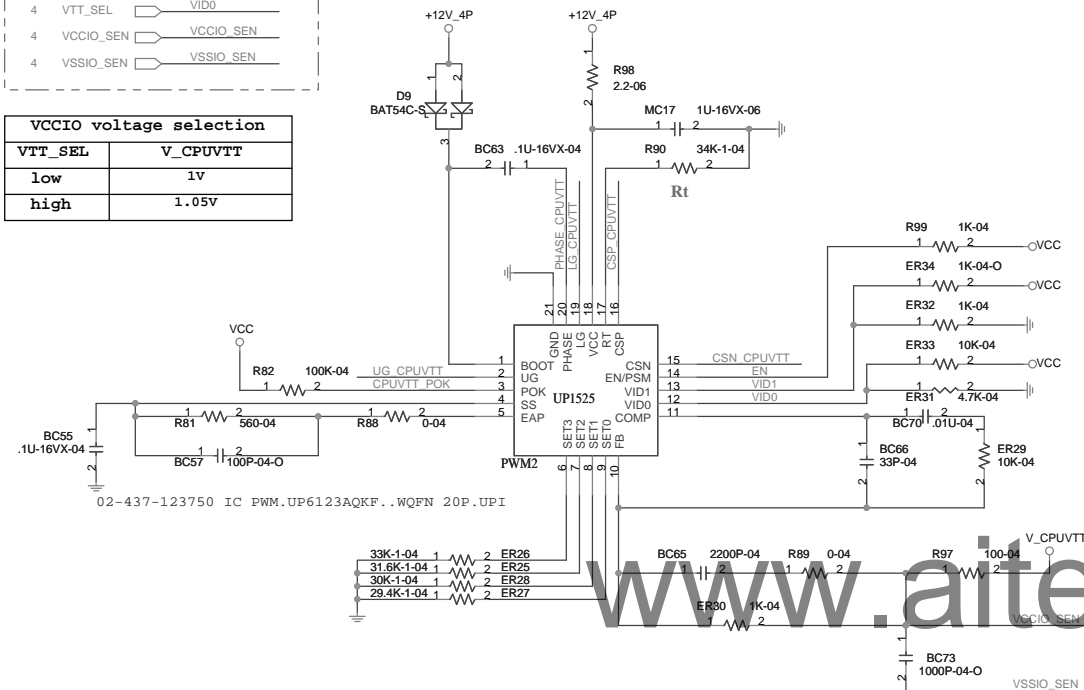


External Connection

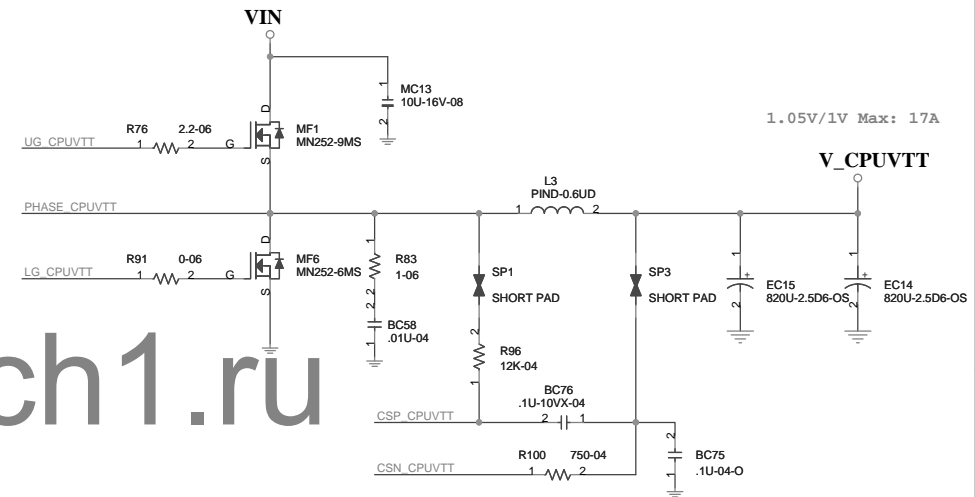
The diagram shows the external connection for the device. It includes the following connections:

- VCC to OVCC
- 3VSB to OV3VSB
- 5VSB to OV5VSB
- V_1P05_PCH to OV_1P05_PCH
- V_CPUVTT to OV_CPUVTT
- VTT_SEL to VID0
- VCCIO_SEN to VCCIO_SEN
- VSSIO_SEN to VSSIO_SEN

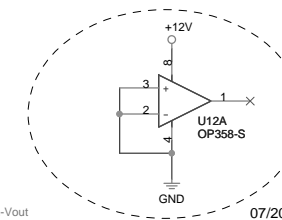
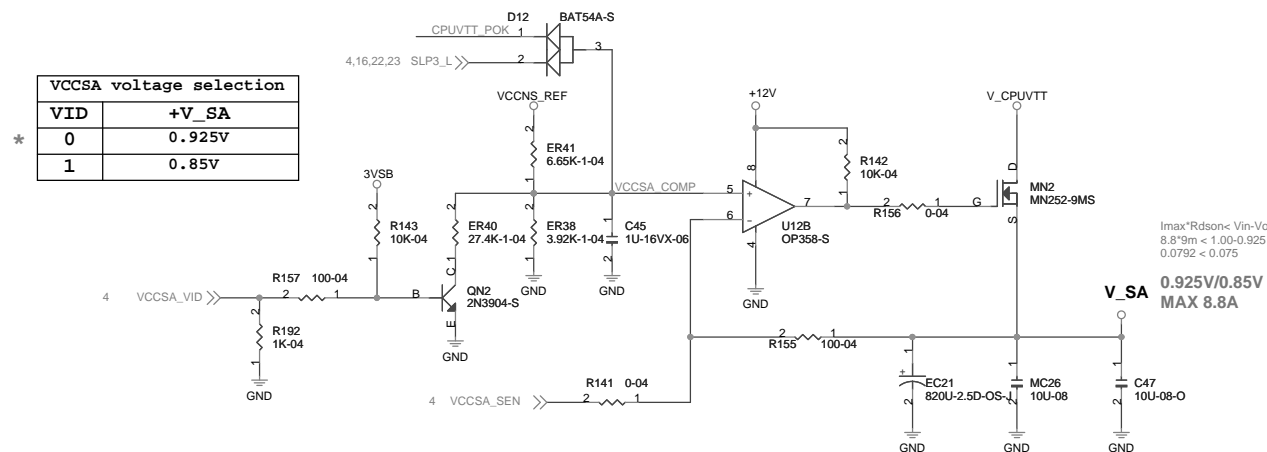
VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
high	1.05V



VID1	VID0	V_CPUVTT
0	0	SET0(1.2V*Rset0/Rt) = 1.0376V
0	1	SET1(1.2V*Rset1/Rt) = 1.0588V
1	0	SET2(1.2V*Rset2/Rt) = 1.1152V
1	1	SET3(1.2V*Rset3/Rt) = 1.1647V



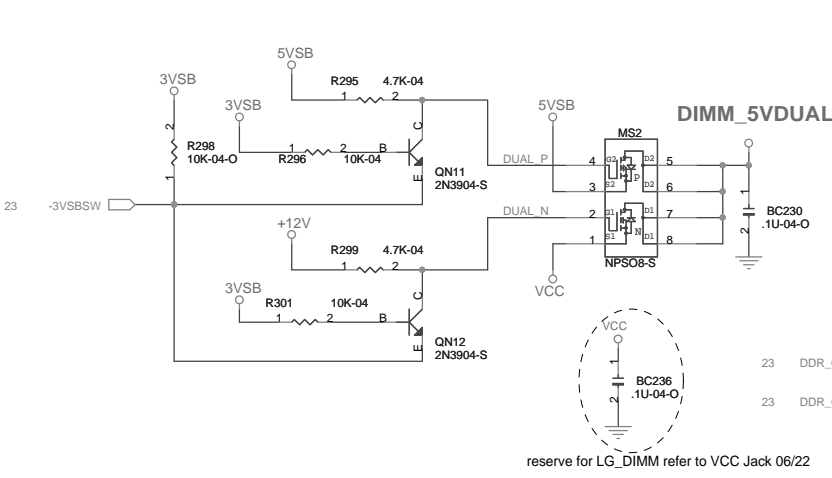
VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V


$$I_{max} \cdot R_{dson} < V_{in} - V_{out}$$

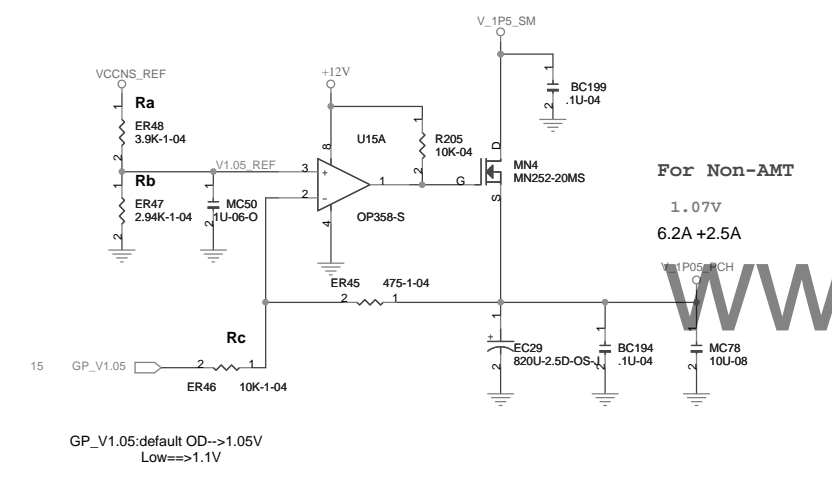
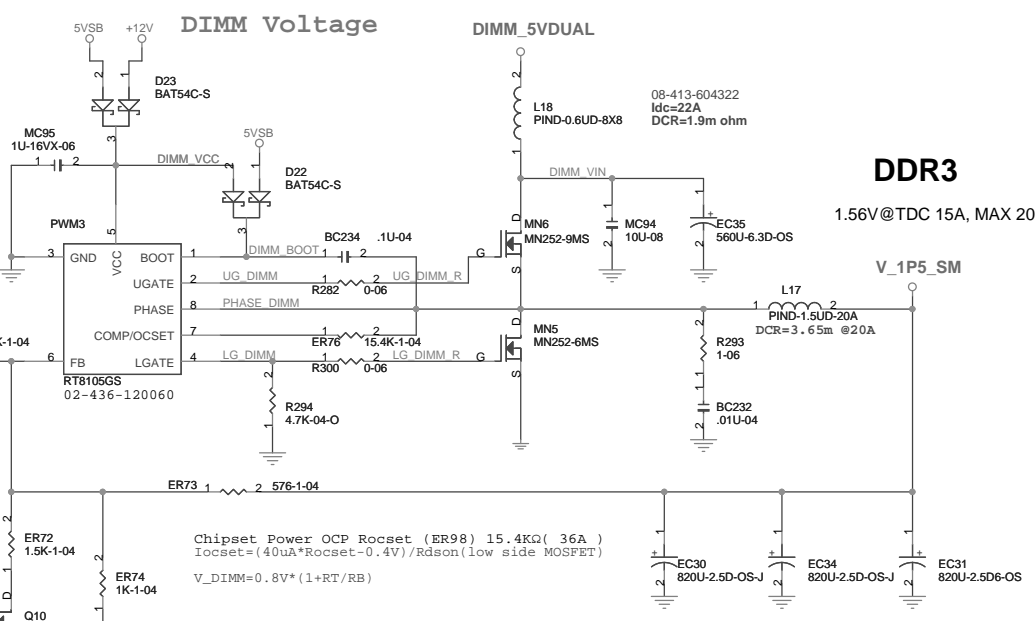
$$8.8 \cdot 9m < 1.00 - 0.925$$

$$0.0792 < 0.075$$

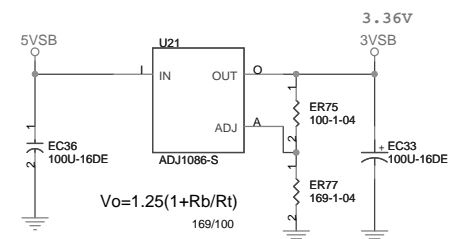
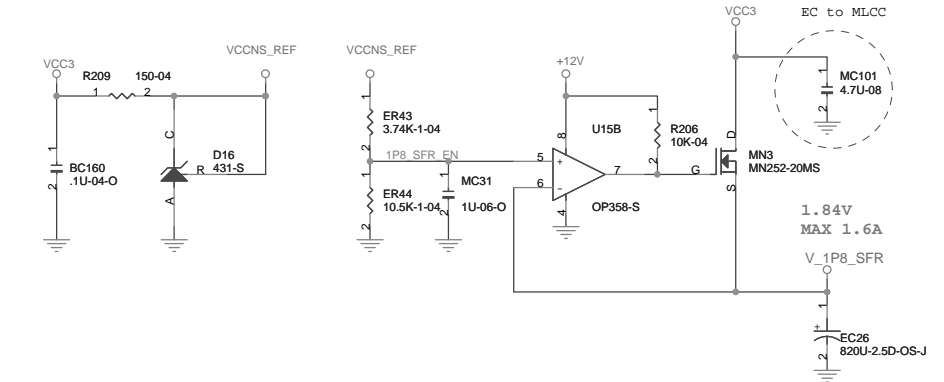
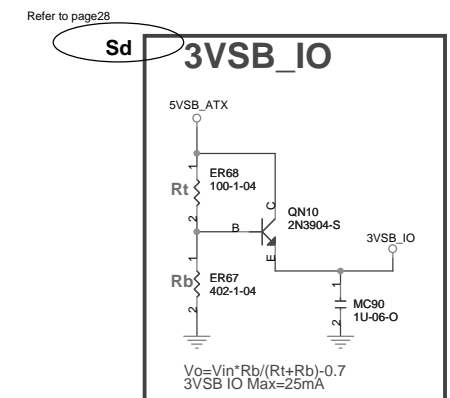
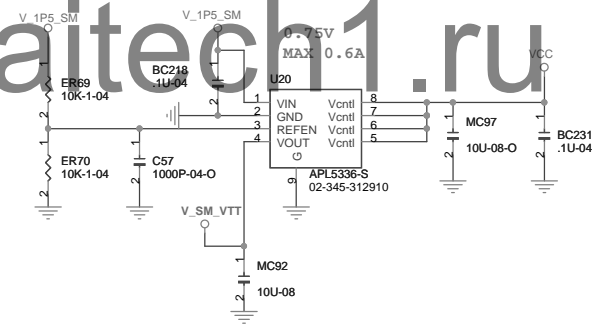
V_SA 0.925V/0.85V
MAX 8.8A



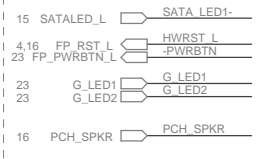
GP63	GP64	V_DIMM
0	1	1.26V
0	0	1.36V
1	1	1.56V
1	0	1.71V



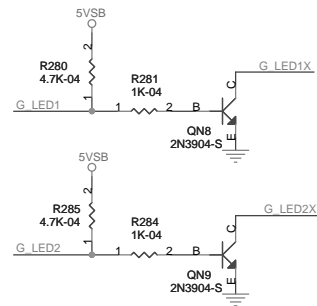
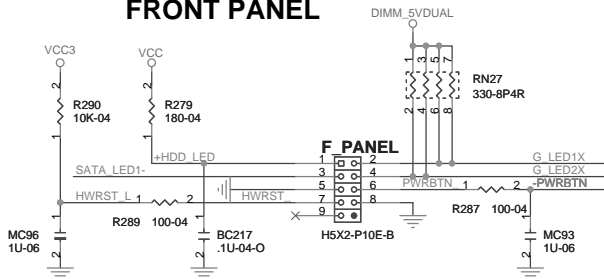
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External Connection

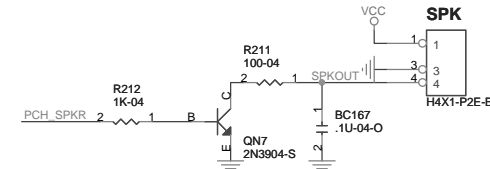


FRONT PANEL



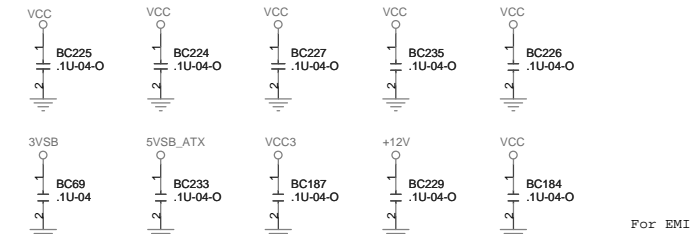
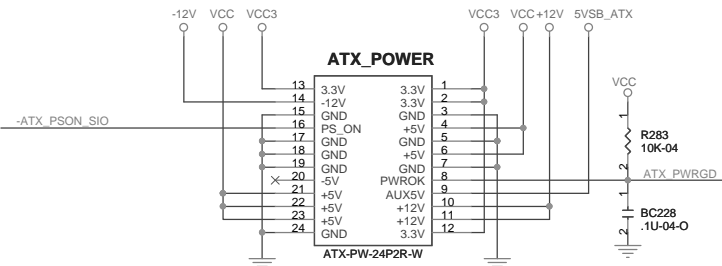
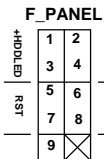
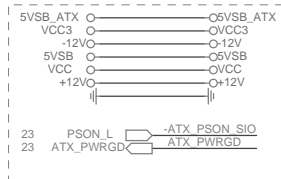
S0	S1	S3	S4	S5
G_LED1	L	B	B	L
G_LED2	H	H	L	L
G	GB	YB	OFF	OFF

B: Blinking



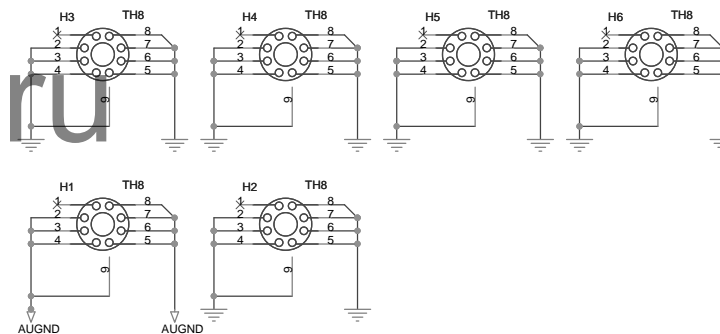
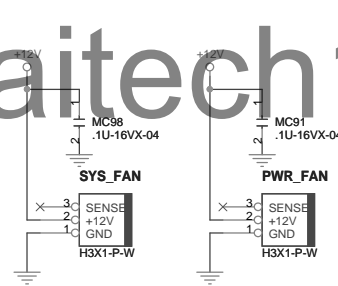
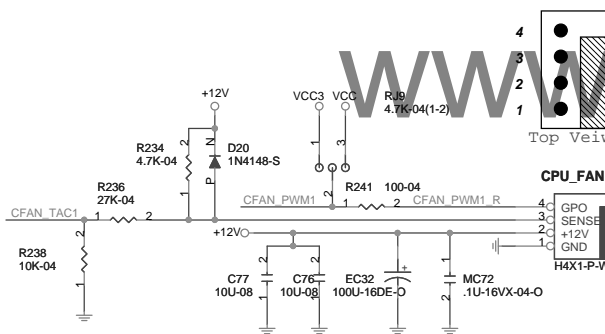
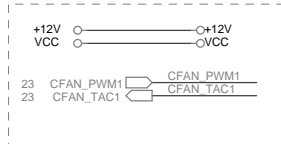
POWER CONNECTOR

External Connection



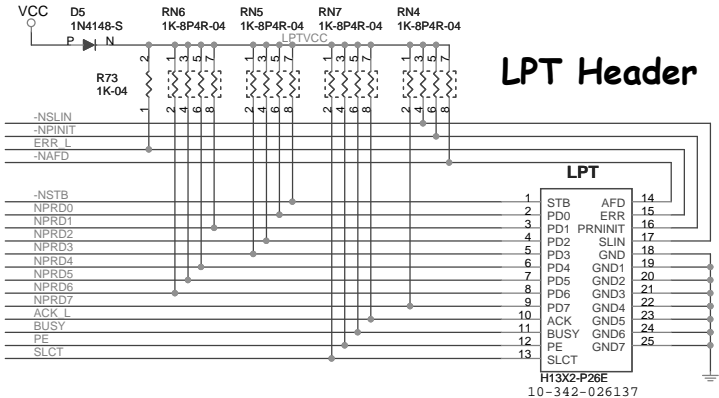
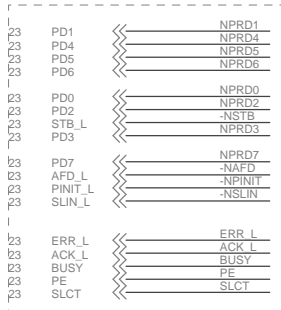
FAN

External Connection

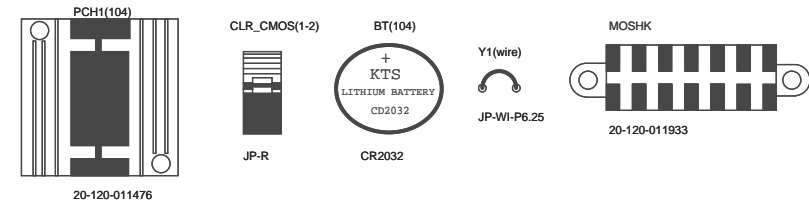


LPT Ports

External Connection



604

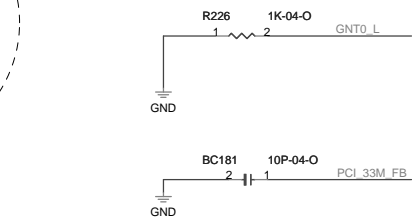
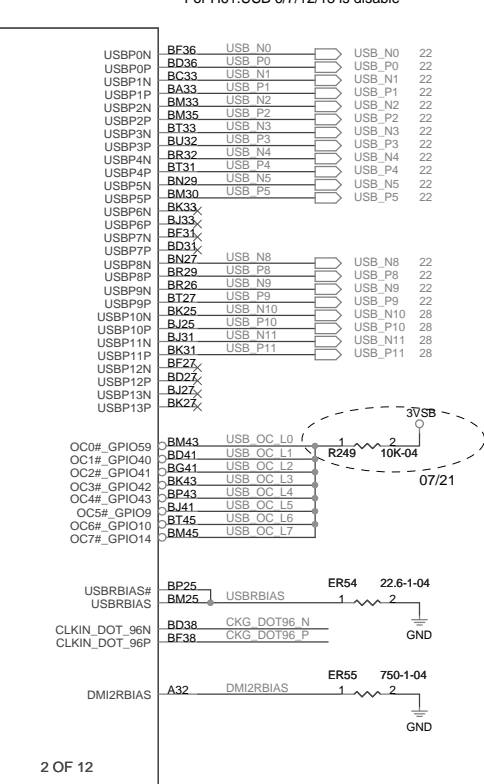
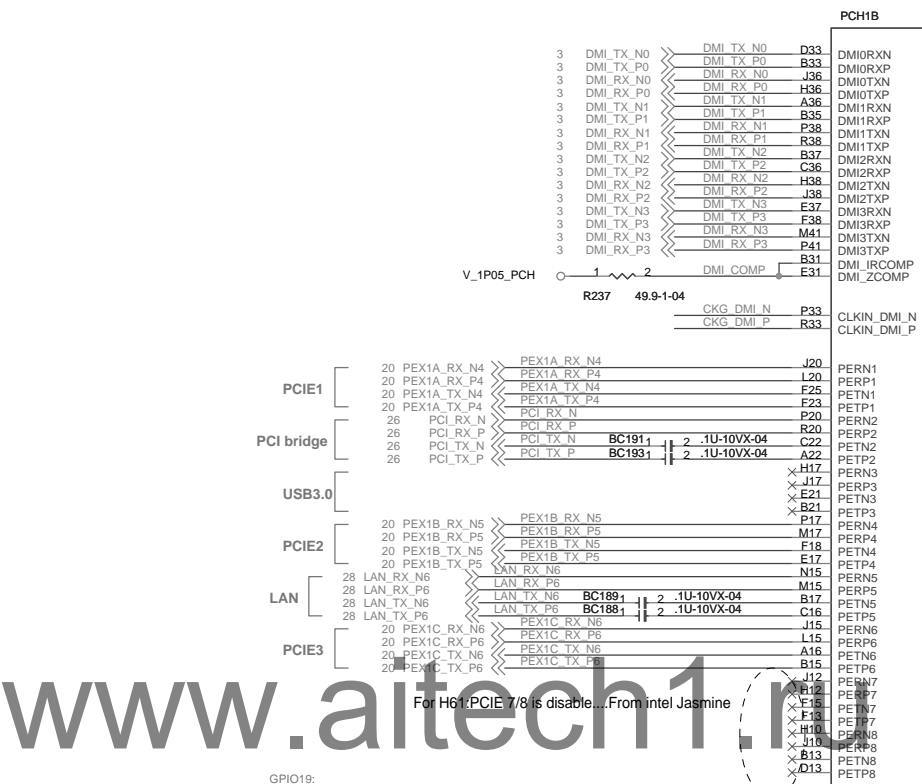


Elitegroup Computer Systems

Title: Front Panel,FAN,PowerConn,GND,104

Size: Document Number H61H2-A Rev 1.0

Date: Wednesday, January 26, 2011 Sheet 13 of 31



Boot Device Select:

BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

*

23 LPC_AD[0..3] L_AD[0..3]

STP46
LPC_AD0 BK15
LPC_AD1 BJ17
LPC_AD2 BJ20
LPC_AD3 BG20
LPC_DRQ0 L BG17
LPC_FRAME L

HDA_BITCLK BJ22
HDA_RST L BC22
HDA_SDI0 BJ22
HDA_SDI1 BJ22
HDA_SDI2 BJ22
HDA_SDI3 BT23
HDA_SDO BT23
HDA_SYNC

SPI_MOSI AU53
SPI_MISO AT55
SPI_CS_L0 AT57
SPI_CLK AR56
SPI_CS_L1 AR56

PCH_RTCX1 BR39
PCH_RTCX2 BR39
RTCST L BT41
SRTCST L BT41
INTRUDER L BM38
PWRGD BJ38
RSMRST L BK38
INTVRMEN BN41
DPWROK BT37
DSWODVREN BR42

SMBALERT L BN49
SMBCLK BT47
SMBDATA BR49
SMLK0ALERT L BU49
SMLK0 LAN CLK BM50
SMLK0 LAN DATA BM50
SMLK1ALERT L BR46
SMLK1 SIO CLK BJ46
SMLK1 SIO_DATA BK46

DSWODVREN R248 390K-04
INTRUDER L R107 1M-04

SMK0 LAN_DATA RN23 2.2K-8P4R-04
SMK0 LAN_CLK 4 3
SMK1 SIO_CLK 6 5
SMK1 SIO_DATA 8 7
PCIE_WAKE L R272 1K-04
PCH_GP30 RN22 8.2K-8P4R-04
PCH_GP27 2 3
PCH_GP31 4 5
PCH_GP45 8 7
SMBALERT L R255 10K-04
SMLK0ALERT L R251 2.2K-04
SMLK1ALERT L R250 10K-04
SMLK1 SIO_CLK R233 10K-04
HDA_SYNC R233 10K-04
PCH_PME L R233 10K-04
RI L RN26 2.2K-8P4R-04
SMBCLK 2 3
SMBDATA 4 5
LPCPD L 8 7

RSMRST L R244 680-04
BC197 1U-04-0

DRAM_PWROK ER58 200-1-04
VCC3

SPI_CS_L1 R260 10K-04
PCH_GP20_PU R275 10K-04
PCH_GP45 R271 10K-04-0
R253 10K-04-0

PCH1D

LDRQ1#_GPIO23
FWH1_LAD0 BK15
FWH1_LAD1 BJ17
FWH2_LAD2 BJ20
FWH3_LAD3 BG20
LDRQ0# BG17
FWH4_LFRAME#

HDA_BCLK
HDA_RST#
HDA_SDI0
HDA_SDI1
HDA_SDI2
HDA_SDI3
HDA_SDO
HDA_SYNC

SPI_MOSI AU53
SPI_MISO AT55
SPI_CS_L0 AT57
SPI_CLK AR56
SPI_CS_L1 AR56

PCH_RTCX1 BR39
PCH_RTCX2 BR39
RTCST L BT41
SRTCST L BT41
INTRUDER L BM38
PWRGD BJ38
RSMRST L BK38
INTVRMEN BN41
DPWROK BT37
DSWODVREN BR42

SMBALERT#_GPIO11
SMBCLK BT47
SMBDATA BR49
SMLK0ALERT#_GPIO60
SMLK0 LAN_CLK BM50
SMLK0 LAN_DATA BM50
SMLK1ALERT#_PCHHOT#_GPIO74
SML1CLK_GPIO68
SML1DATA_GPIO75

DSWODVREN R248 390K-04
INTRUDER L R107 1M-04

U1CPT

BMBUSY#_GPIO0
CLKRUN#_GPIO32
HDA_DOCK_EN#_GPIO33
STP_PCI#_GPIO35
GPIO35

GPIO8
LAN_PHY_PWR_CTRL#_GPIO12
HDA_DOCK_RST#_GPIO13
GPIO15
GPIO28
SLP_LAN#_GPIO29
PCIECLKRQ2#_GPIO20
PCIECLKRQ5#_GPIO44
PCIECLKRQ6#_GPIO45
PCIECLKRQ7#_GPIO46
GPIO57
SYS_PWROK

SPI_MOSI AU53
SPI_MISO AT55
SPI_CS_L0 AT57
SPI_CLK AR56
SPI_CS_L1 AR56

PCH_RTCX1 BR39
PCH_RTCX2 BR39
RTCST L BT41
SRTCST L BT41
INTRUDER L BM38
PWRGD BJ38
RSMRST L BK38
INTVRMEN BN41
DPWROK BT37
DSWODVREN BR42

SMBALERT#_GPIO11
SMBCLK BT47
SMBDATA BR49
SMLK0ALERT#_GPIO60
SMLK0 LAN_CLK BM50
SMLK0 LAN_DATA BM50
SMLK1ALERT#_PCHHOT#_GPIO74
SML1CLK_GPIO68
SML1DATA_GPIO75

DSWODVREN R248 390K-04
INTRUDER L R107 1M-04

U1CPT

AW55_SMIUSB3
BC56_CLKRUN L
BC25_HDA_DOCK_EN L
BL56_FP_AUD_DETECT
BJ57_TP_GPIO35

GPIO8
LAN_PHY_PWR_CTRL#_GPIO12
HDA_DOCK_RST#_GPIO13
GPIO15
GPIO28
SLP_LAN#_GPIO29
PCIECLKRQ2#_GPIO20
PCIECLKRQ5#_GPIO44
PCIECLKRQ6#_GPIO45
PCIECLKRQ7#_GPIO46
GPIO57
SYS_PWROK

SPI_MOSI AU53
SPI_MISO AT55
SPI_CS_L0 AT57
SPI_CLK AR56
SPI_CS_L1 AR56

PCH_RTCX1 BR39
PCH_RTCX2 BR39
RTCST L BT41
SRTCST L BT41
INTRUDER L BM38
PWRGD BJ38
RSMRST L BK38
INTVRMEN BN41
DPWROK BT37
DSWODVREN BR42

SMBALERT#_GPIO11
SMBCLK BT47
SMBDATA BR49
SMLK0ALERT#_GPIO60
SMLK0 LAN_CLK BM50
SMLK0 LAN_DATA BM50
SMLK1ALERT#_PCHHOT#_GPIO74
SML1CLK_GPIO68
SML1DATA_GPIO75

DSWODVREN R248 390K-04
INTRUDER L R107 1M-04

U1CPT

TP21
TP47
TP24

GPIO8
LAN_PHY_PWR_CTRL#_GPIO12
HDA_DOCK_RST#_GPIO13
GPIO15
GPIO28
SLP_LAN#_GPIO29
PCIECLKRQ2#_GPIO20
PCIECLKRQ5#_GPIO44
PCIECLKRQ6#_GPIO45
PCIECLKRQ7#_GPIO46
GPIO57
SYS_PWROK

SPI_MOSI AU53
SPI_MISO AT55
SPI_CS_L0 AT57
SPI_CLK AR56
SPI_CS_L1 AR56

PCH_RTCX1 BR39
PCH_RTCX2 BR39
RTCST L BT41
SRTCST L BT41
INTRUDER L BM38
PWRGD BJ38
RSMRST L BK38
INTVRMEN BN41
DPWROK BT37
DSWODVREN BR42

SMBALERT#_GPIO11
SMBCLK BT47
SMBDATA BR49
SMLK0ALERT#_GPIO60
SMLK0 LAN_CLK BM50
SMLK0 LAN_DATA BM50
SMLK1ALERT#_PCHHOT#_GPIO74
SML1CLK_GPIO68
SML1DATA_GPIO75

DSWODVREN R248 390K-04
INTRUDER L R107 1M-04

U1CPT

Buffer Through Mode / Integrated Clock Mode have been changed to F/W Strap. Default: Integrated Clock Mode. Doc. Cougar Point Platform Controller Hub (PCH) Family EDS Update V0.7.1

IGC EN L R252 1K-04

Integrated Clock:

IGC_EN L (internal PU)	
H	Buffer Through Mode
L	Integrated Clock Mode

In Sugar Bay Q series Platform, Enable TLS for vPro.

TLS EN

TLS Confidentiality:

TLS_EN (internal PD)	
H	Enable TLS
L	Disable TLS

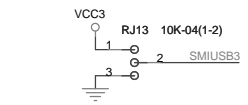
PCH_SPKR

No Reboot:

PCH_SPKR (internal PD)	
H	Enable No Reboot
L	Disable

INTVRMEN

H	Enable
L	Disable

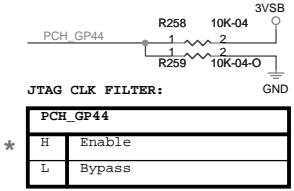


- When Deep Sleep not implemented:
- 1.PCH_GP30, PCH_GP27 need to be Pull Up.
 - 2.VCC3SW3_3 should to be connected to +3VSB.
 - 3.SLP_SUS_L, SUSACK_L left unconnected.
 - 4.SUSWARN_L may be used as GPIO30.(Reference to 1.)

R245 0-04 DPWROK

RSMRST L	DPWROK
----------	--------

For platform not supporting deep sleep connect directly to RSMRST#.



PCH_GP46

DFX TEST MODE Rings Oscillator:

PCH_GP46 (internal PU)	
H	Enable
L	Bypass

ON DIE PLL EN

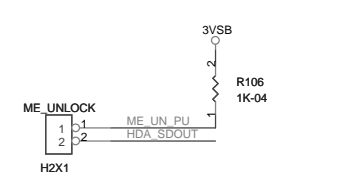
On-Die PLL VR:

ON_DIE_PLL_EN (internal PU)	
H	Enable
L	Disable

HDA_SYNC

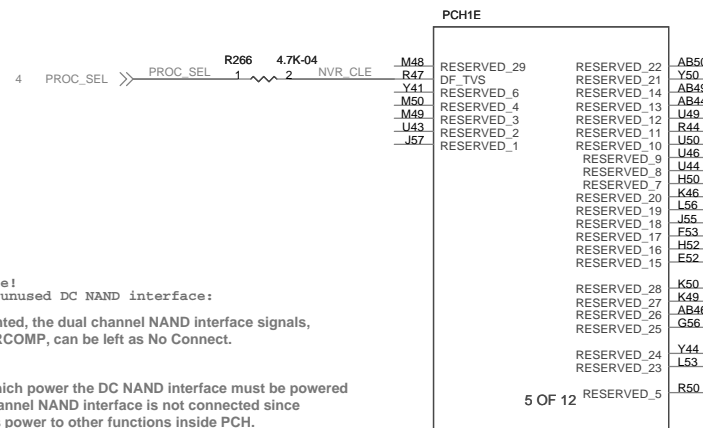
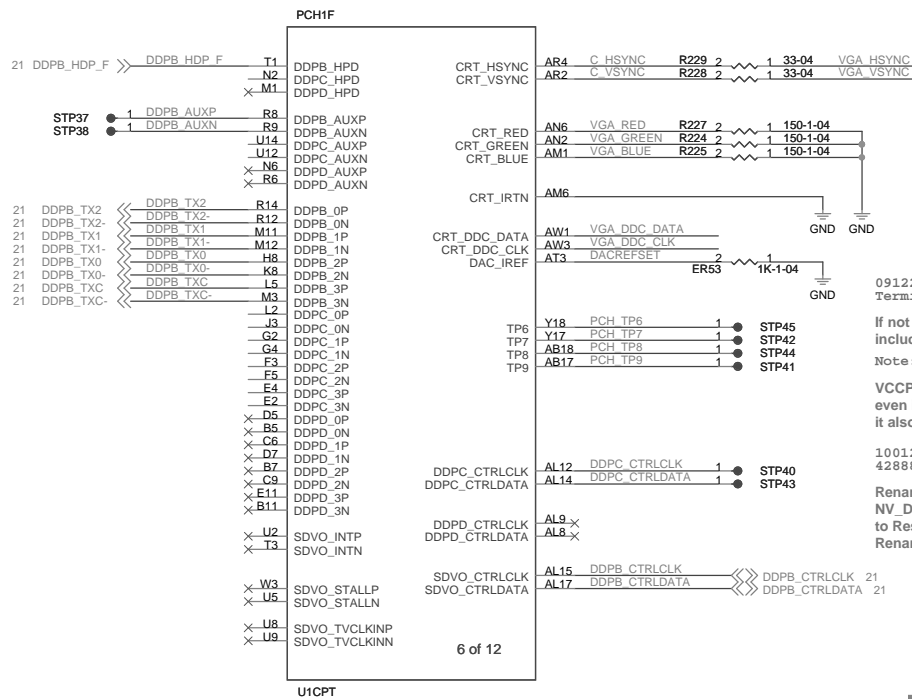
On-Die PLL VR Source:

HDA_SYNC_R (internal PD)	
H	1.5V
L	1.8V



ME Enable/Disable

ME_UNLOCK	ME_UNLOCK
1-2	UNLOCK
Float	LOCK



091222 Update!
Terminating unused DC NAND interface:

If not implemented, the dual channel NAND interface signals, including NV_RCOMP, can be left as No Connect.

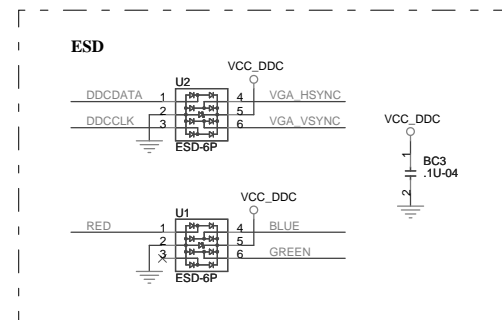
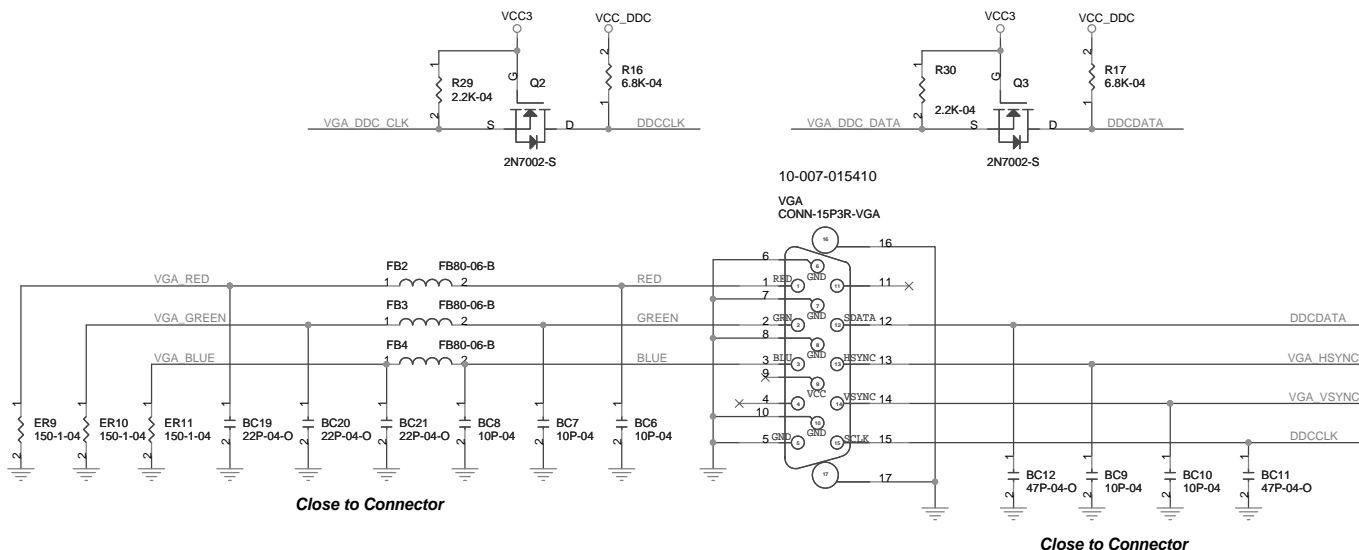
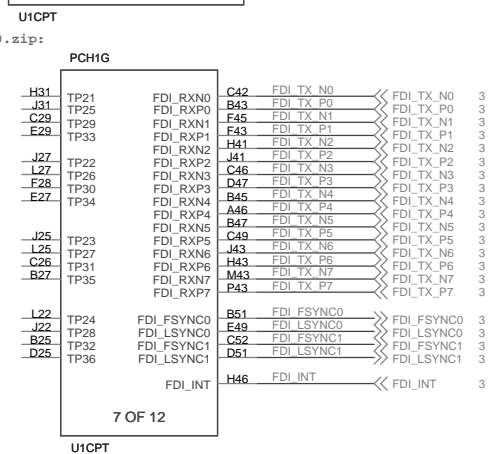
Note:

VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.

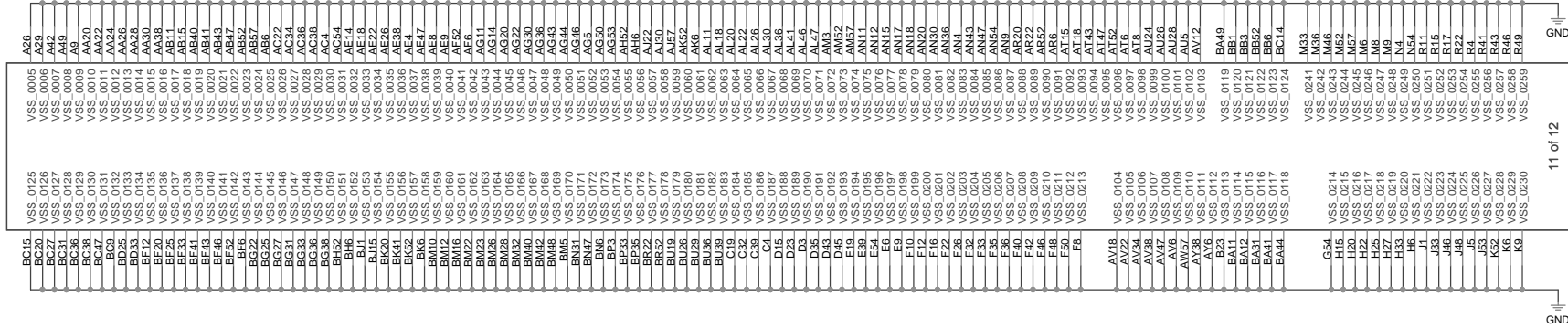
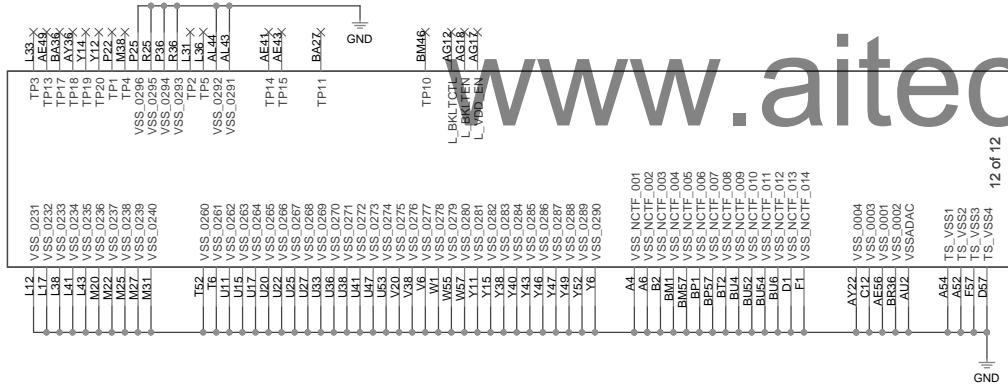
100120 Update!
428880_428880_Cougar_Point_Desktop_Ballout_Mech_Package_Rev1p0.zip:

Renamed NV_WE#_CK[0:1], NV_RE#_WRB[0:1], NV_RCOMP, NV_RB#, NV_DQ9 / NV_IO[0:15], NV_DQS[0:1], NV_CE#[0:3], and NV_ALE to Reserved(RSVD).

Renamed NV_CLE to DF_TVSS.



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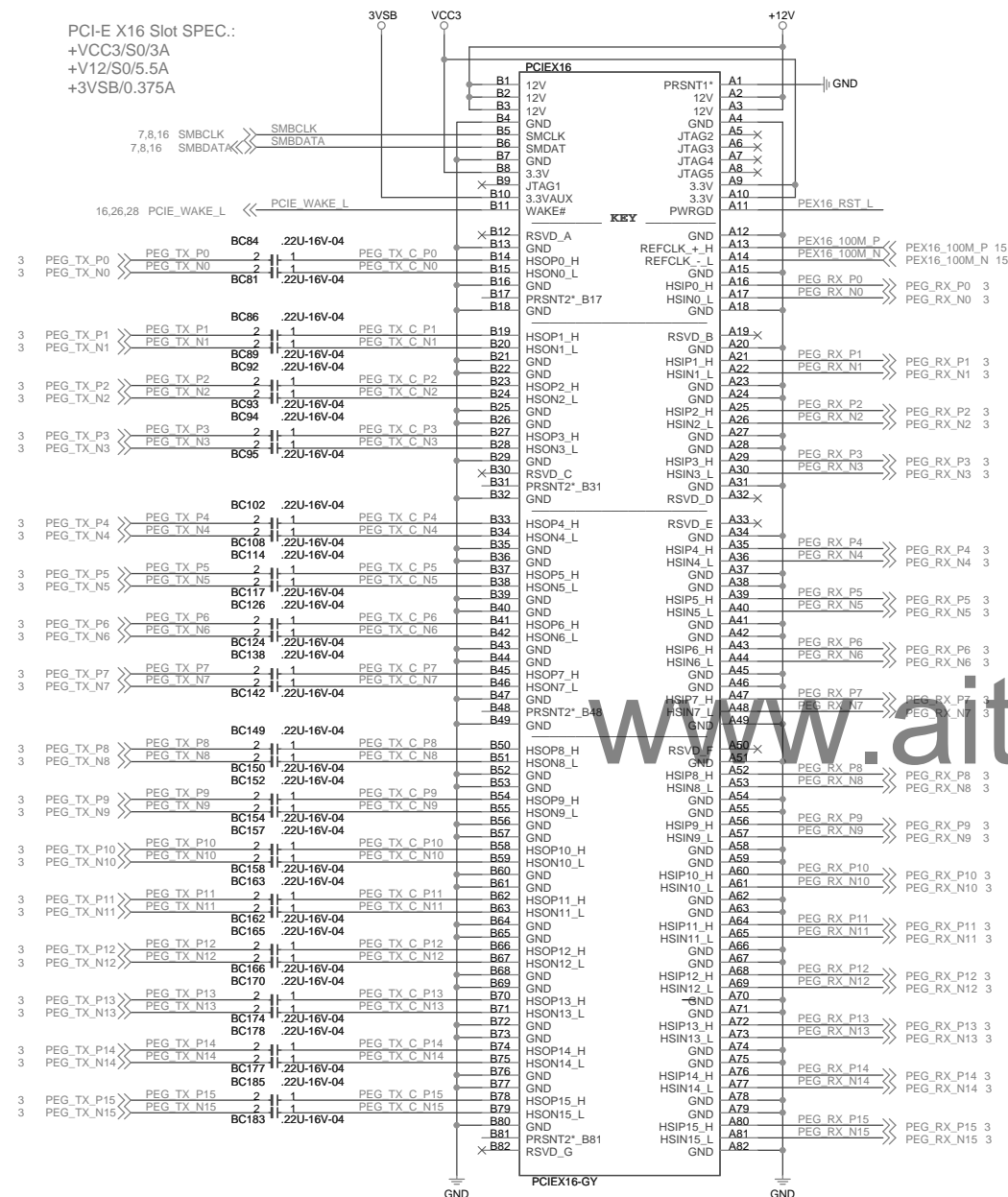
Title		PCH - GND	
Size	Document Number	H61H2-A	
Custom		Rev 1.0	
Date:	Wednesday, January 26, 2011	Sheet	19 of 31

PCI-E X16 Slot SPEC.:

+VCC3/S0/3A

+V12/S0/5.5A

+3VSB/0.375A

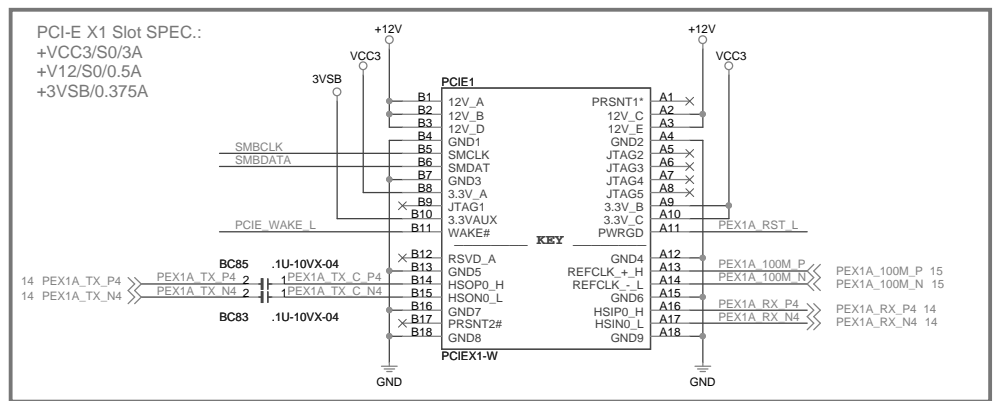


PCI-E X1 Slot SPEC.:

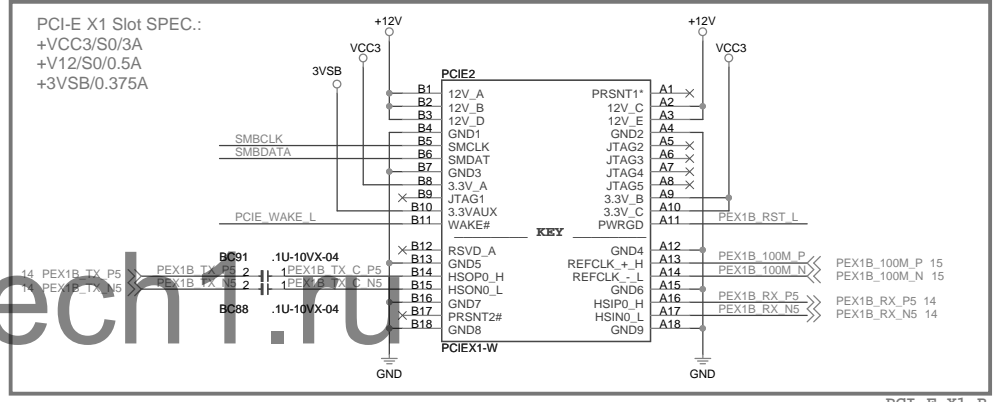
+VCC3/S0/3A

+V12/S0/0.5A

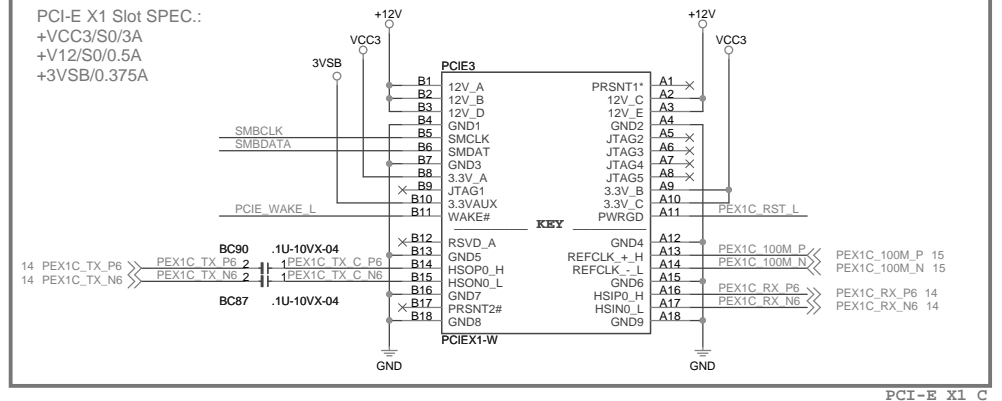
+3VSB/0.375A



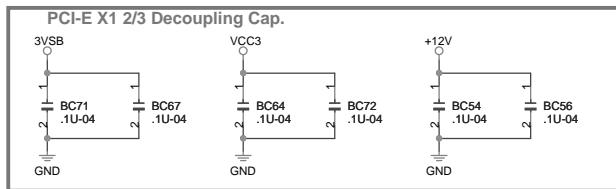
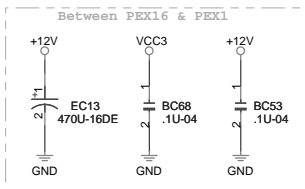
PCI-E X1 A



PCI-E X1 B

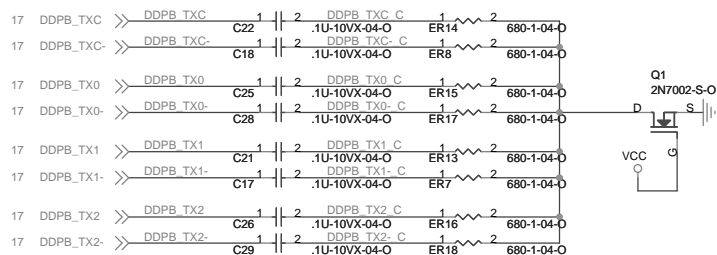


PCI-E X1 C

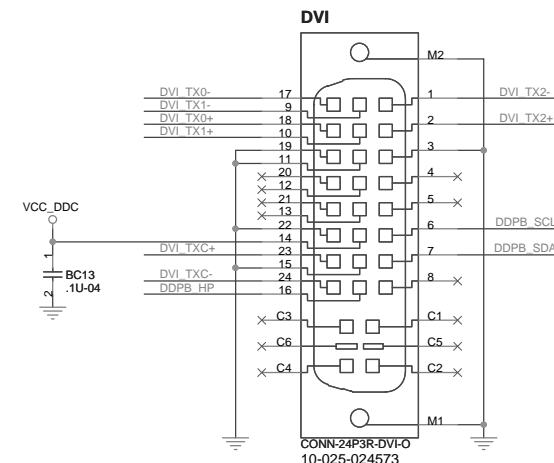
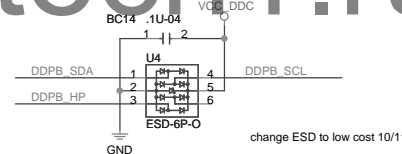
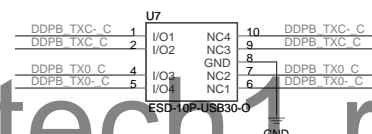
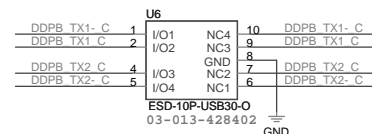
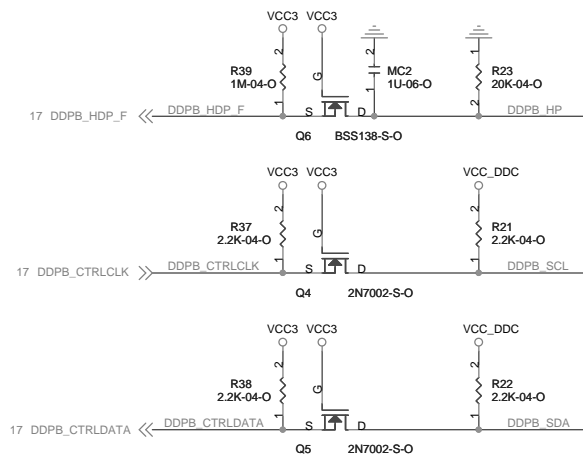
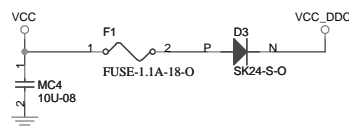
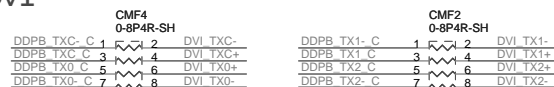


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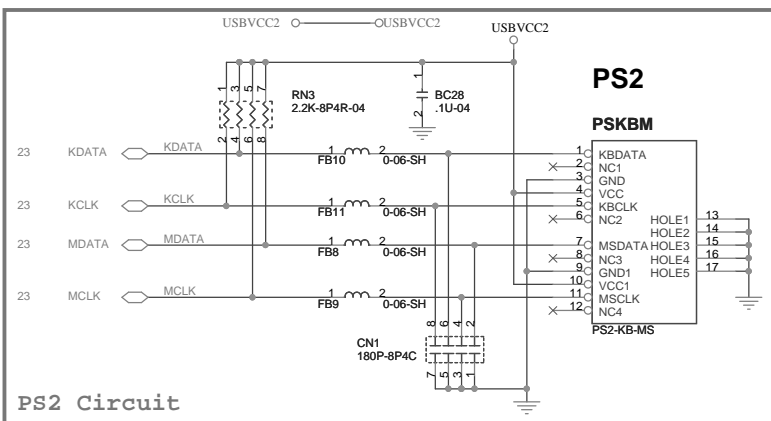
Title		Slot - PCI-EX16/PCI-EX1	
Size	Document Number	H61H2-A	
Customer	Rev 1.0		
Date:	Wednesday, January 26, 2011	Sheet	20 of 31



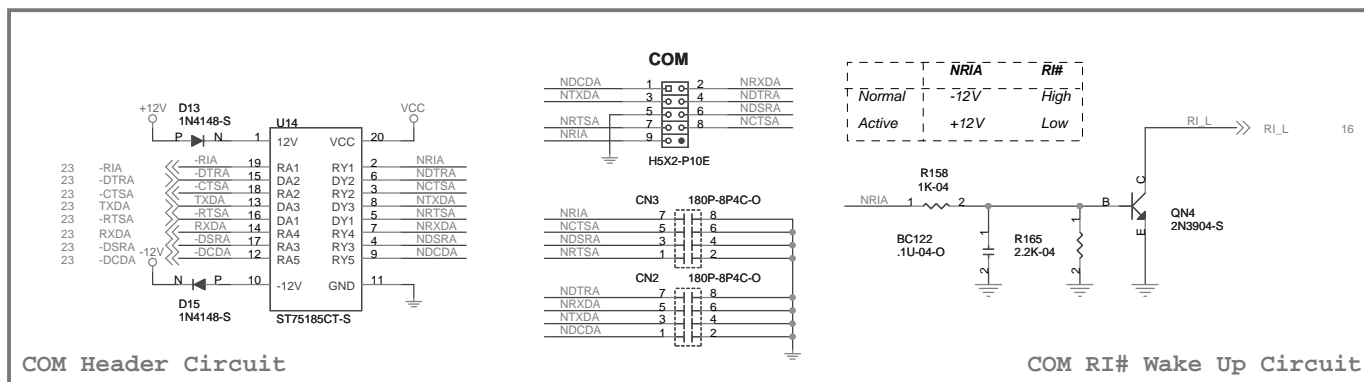
DVI



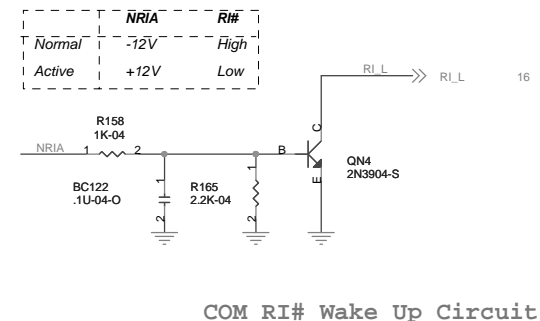
www.aitech1.ru



PS2 Circuit



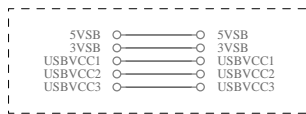
COM Header Circuit



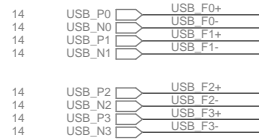
COM RI# Wake Up Circuit

ECS Elitegroup Computer Systems

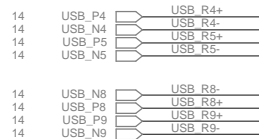
Title		DVI&HDMI CONN&COM&PS2	
Size	Document Number	H61H2-A	
Custom		Rev 1.0	
Date:	Wednesday, January 26, 2011	Sheet	21 of 31



USB FRONT SIDE



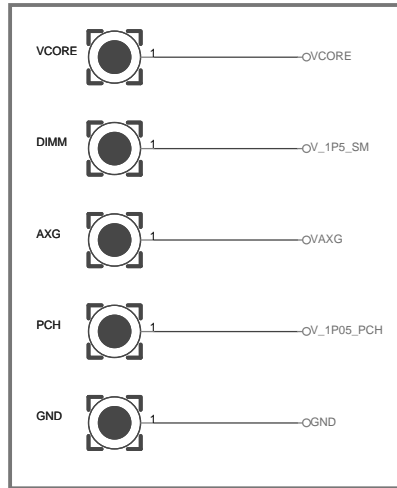
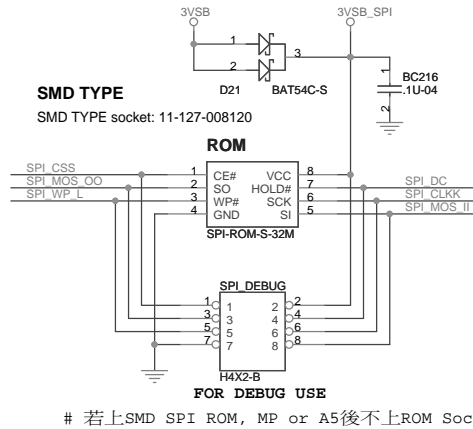
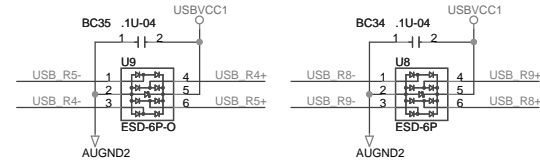
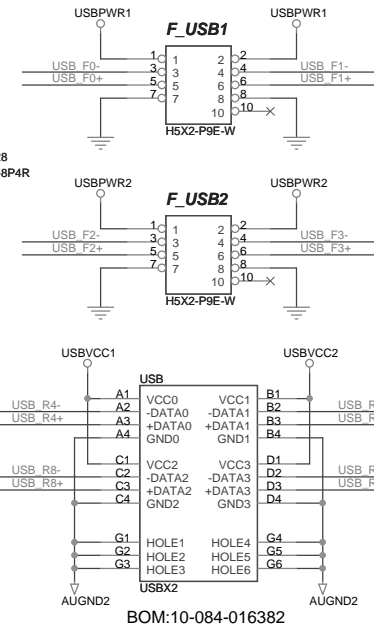
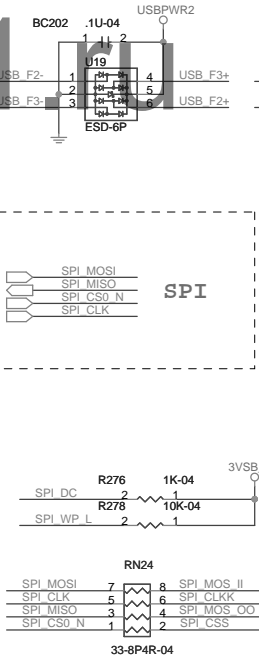
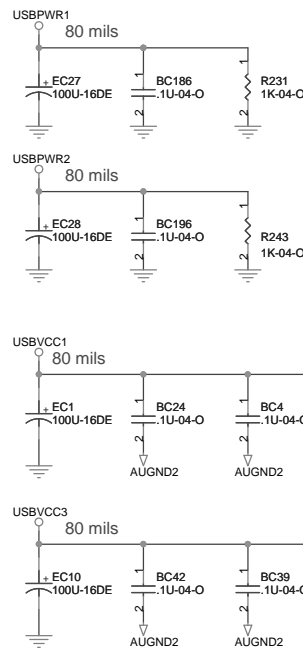
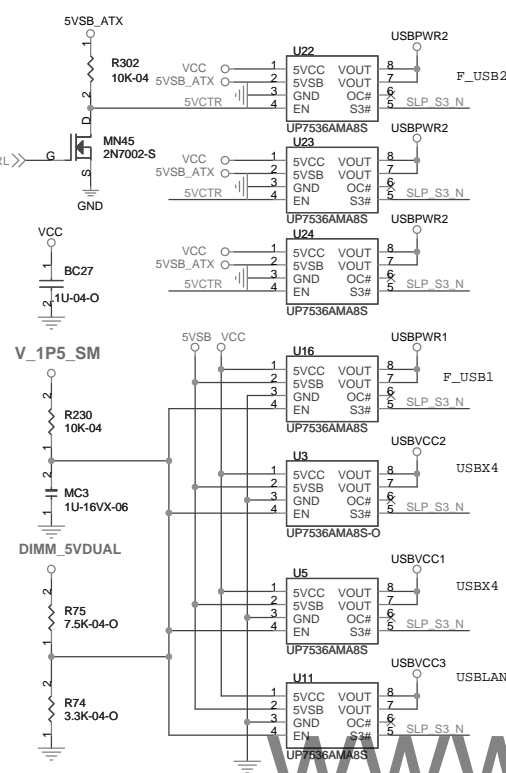
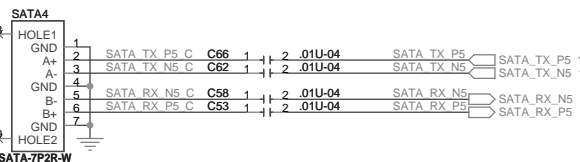
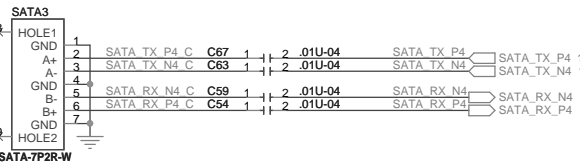
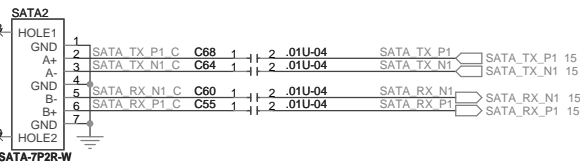
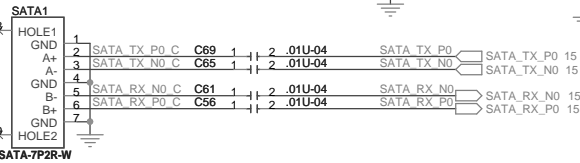
REAR SIDE



4,11,16,23 SLP3_L SLP3_N



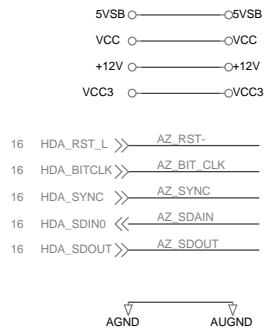
Layout Note:
SATA3.0 4.5/7.5/20 in 90 Ω ±17.5%
SATA2.0 4.5/7.5/15 in 90 Ω ±17.5%



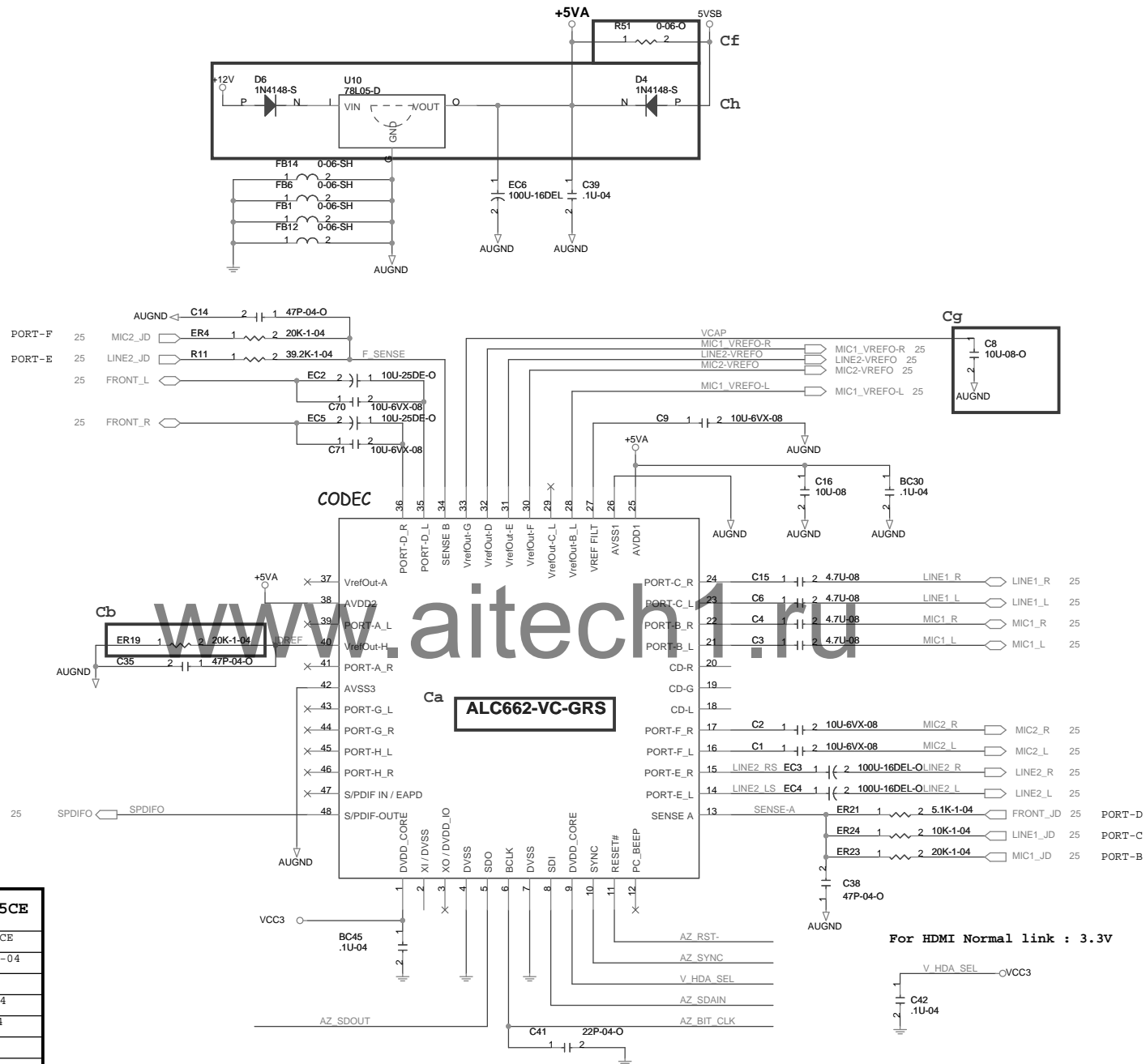
ELI Measure Point

Title		
USB/SATA/SPI		
Size	Document Number	Rev
Custom	H61H2-A	1.0
Date:	Thursday, January 27, 2011	Sheet 22 of 31

External Connection



* VCC1.5 can remove for non-Intel G4X platform



BOM Difference

Location	ALC662	VT1705	VT1705CE
Ca	ALC662-VC-GRS	VT1705	VT1705CE
Cb	20K-1-04	5.1K-1-04	5.1K-1-04
Cc	V	X	X
Cd	2.2K-04	3.3K-04	3.3K-04
Ce	75-04	75-04	75-04
Cf	X	X	V
Cg	X	X	V
Ch	V	V	X

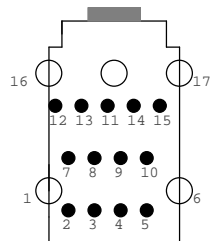
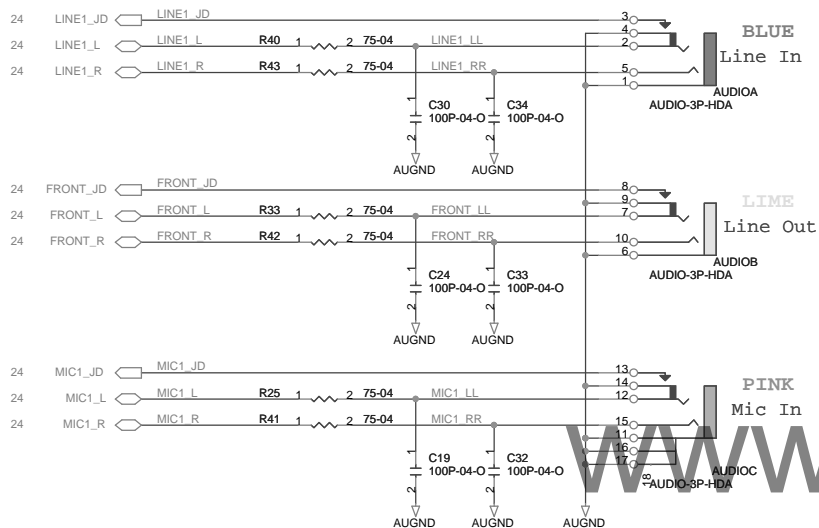
When you change BOM, remember change GPI to inform BIOS use different Verb-Table.

External Connection

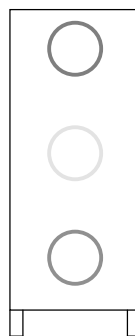
16 FP_AUD_DETECT <-- FP_AUD_DETECT

* HDPANEL_DETECT connect to SIO or SB GPIO
for AC97 Panel support

REAR-AUDIO Non re-tasking for rear panel

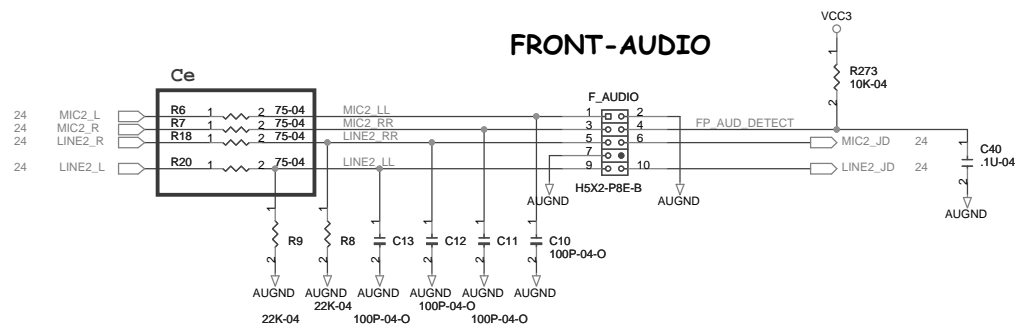


TOP VIEW

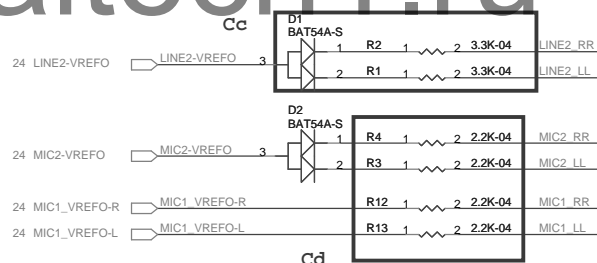


FRONT VIEW

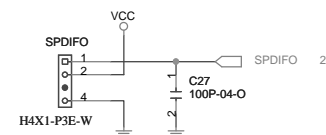
FRONT-AUDIO



MIC Bias



SPDIF-OUT



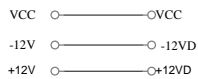
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Title: **AUDIO VT1705/ALC662 (PANEL)**

Size: Custom Document Number: **H61H2-A** Rev: **1.0**

Date: Wednesday, January 26, 2011 Sheet 25 of 31

External Connection



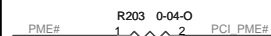
COMMON

26	PAD[31:0]	PAD[31:0]
26	PCIRST#	PCIRST#
26	PCBE0#	PCBE0#
26	PCBE1#	PCBE1#
26	PCBE2#	PCBE2#
26	PCBE3#	PCBE3#
26	PME#	PME#
26	PM66EN	PM66EN
26	PFRAME#	PFRAME#
26	PIRDY#	PIRDY#
26	PSTOP#	PSTOP#
26	PDVSEL#	PDVSEL#
26	PPAR	PPAR
26	PSERR#	PSERR#
26	PPERR#	PPERR#
26	PCICLK0	PCICLK0
26	PLOCK#	PLOCK#
26	PINTA#	PINTA#
26	PINTB#	PINTB#
26	PINTC#	PINTC#
26	PINTD#	PINTD#
26	PREQ0#	PREQ0#
26	PGNT0#	PGNT0#
26	PCICLK1	PCICLK1
26	PREQ1#	PREQ1#
26	PGNT1#	PGNT1#

14	PCHINTA_L	PCHINTA_L
14	PCHINTB_L	PCHINTB_L
14	PCHINTC_L	PCHINTC_L
14	PCHINTD_L	PCHINTD_L
14	PCH_PME_L	PCH_PME_L

PCI CHIP

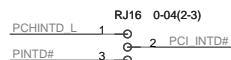
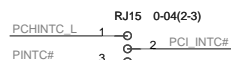
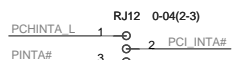
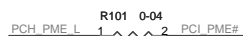
Se For page 26



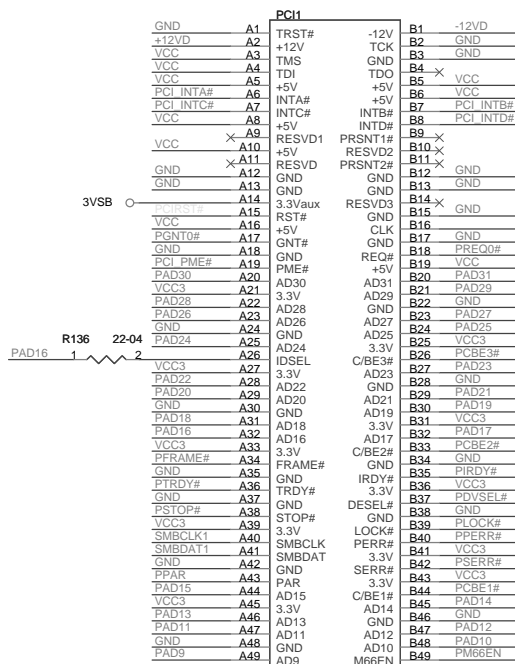
For ITE chipset auto power-on issue.

As document WW32 2010 Sandy Bridge and Cougar Point Based Platforms Field Message of the Week

Reserve for Intel PCI Legacy

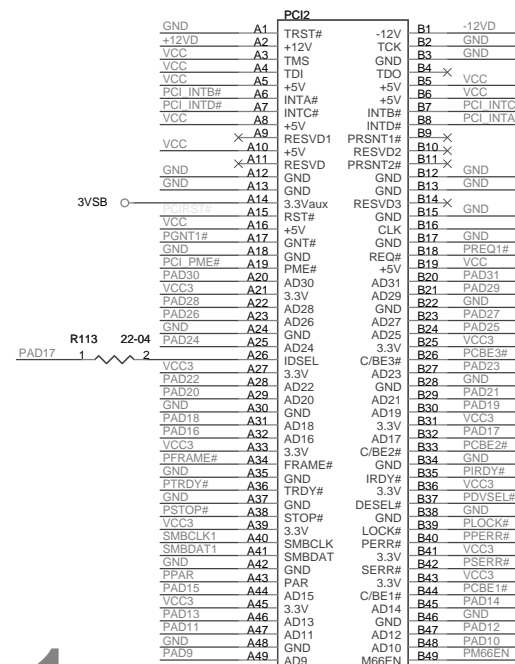


PCI1



PCI-W

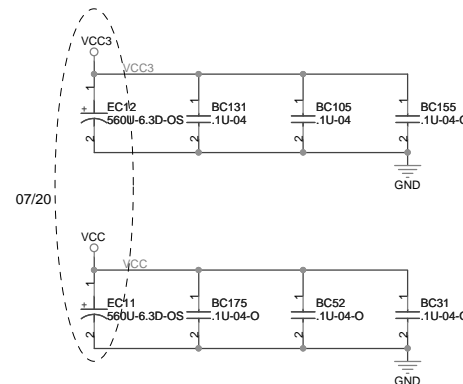
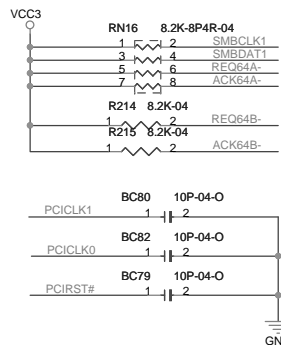
PCI2



PCI-W

PCI1:REQ0;GNT0 IDSEL:16 INT:ABCD

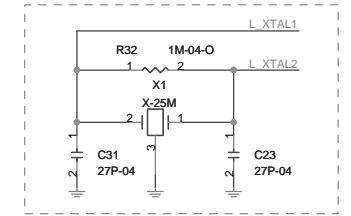
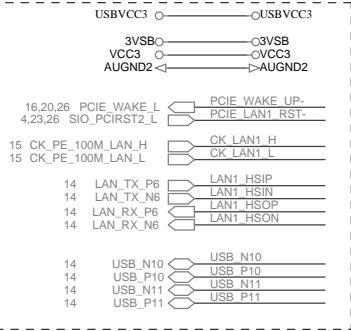
PCI2:REQ1;GNT1 IDSEL:17 INT:BCDA



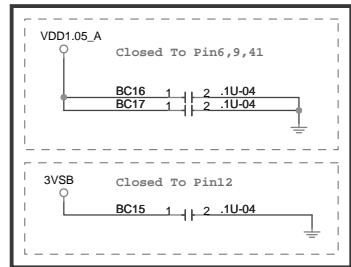
Elitegroup Computer Systems

Title	Slot - PCI1 & PCI2
Size	Document Number
Custom	H61H2-A
Date	Wednesday, January 26, 2011
Sheet	27 of 31
Rev	1.0

External Connection



Cb



BOM Difference

	RTL8111E-VL-CG 1000M	RTL8105E-GR 10/100M
Ca	RTL8111E-VB-GR	RTL8105E-GR
Cb	V	X
Cc	USBX2-LAN-1000	USBX2-LAN-100
Cd	X	V
Ce	0-04	.01U-25VX-04
Cf	V	X
Cg	USBX2-LAN-1000	USBX2-LAN-100

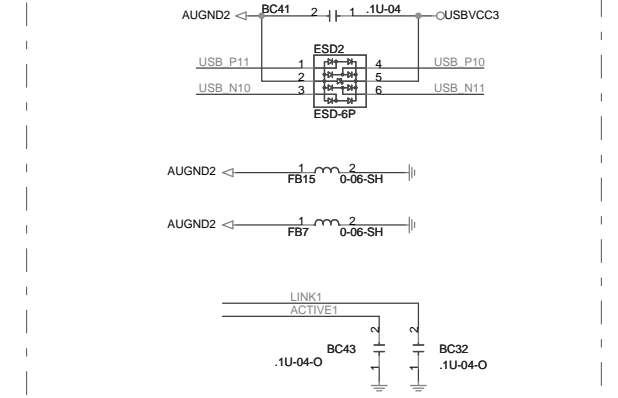
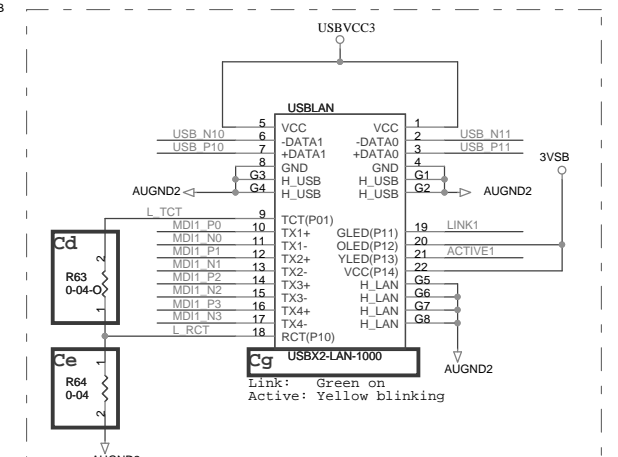
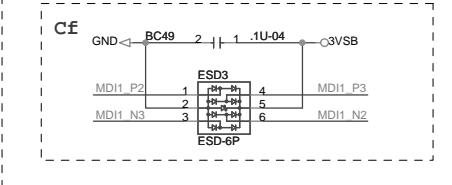
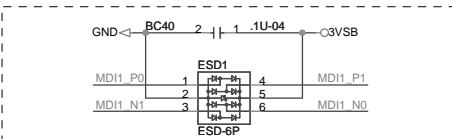
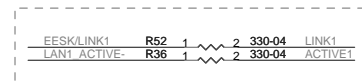
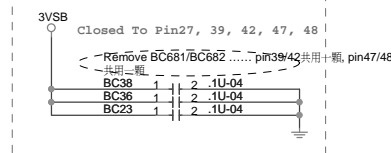
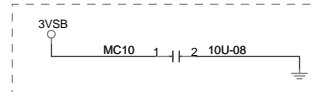
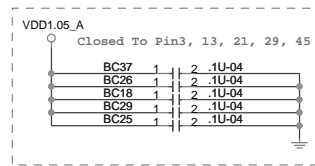
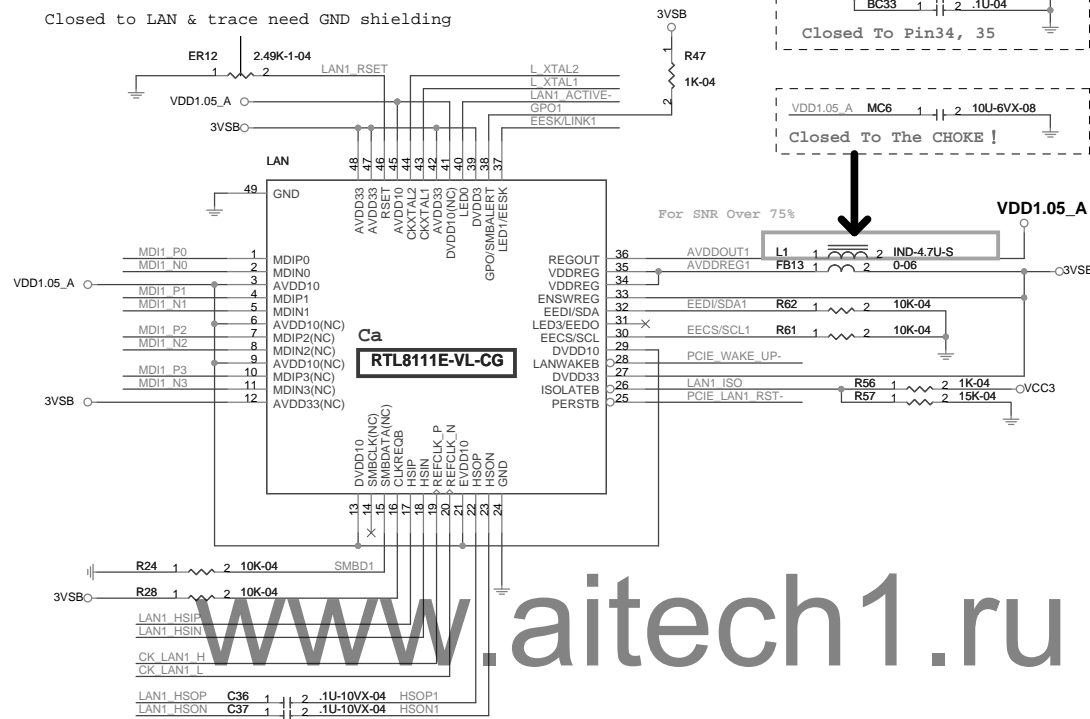
新手提醒:

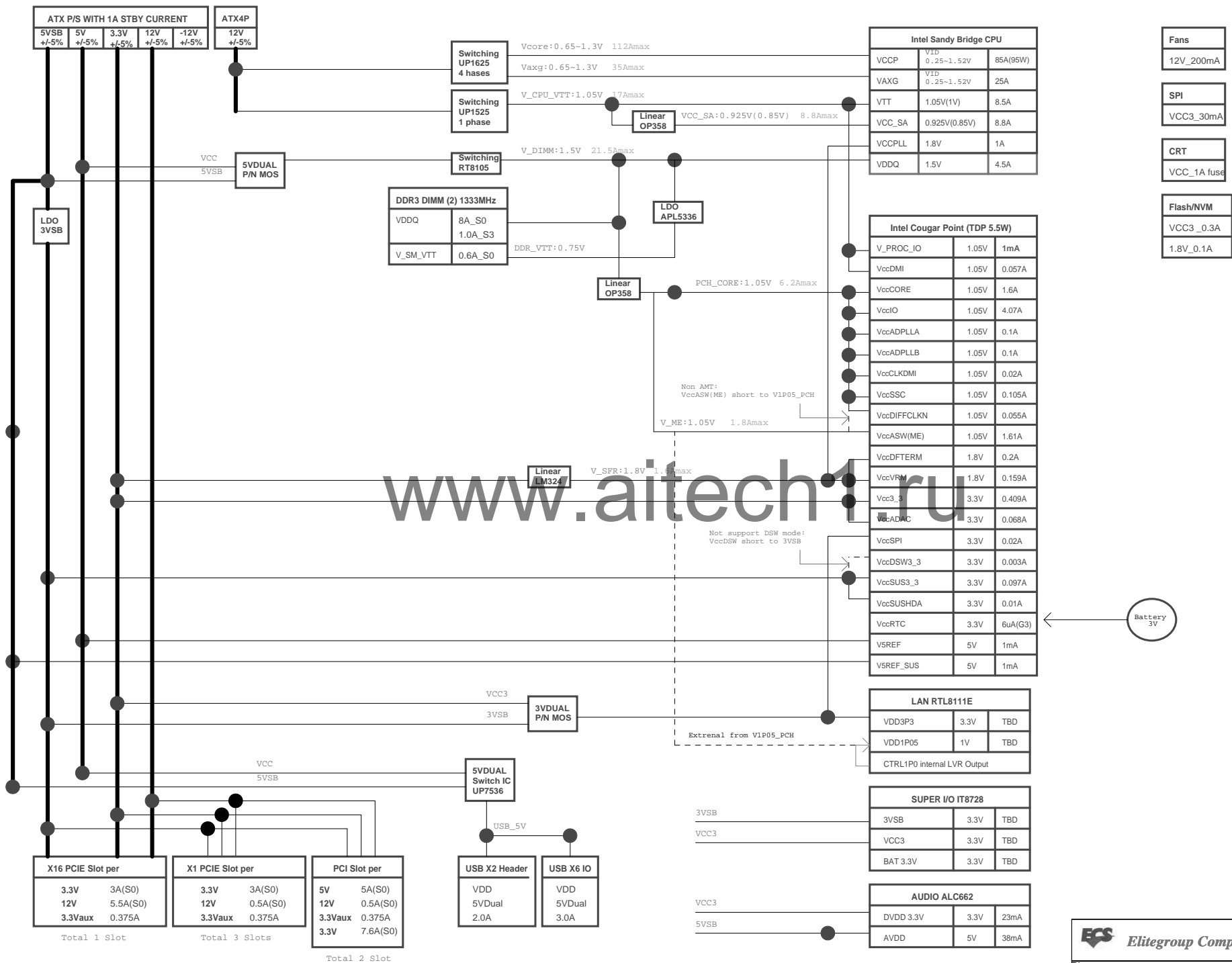
LAN_HSOP/N請接到SB的PCIE RX端

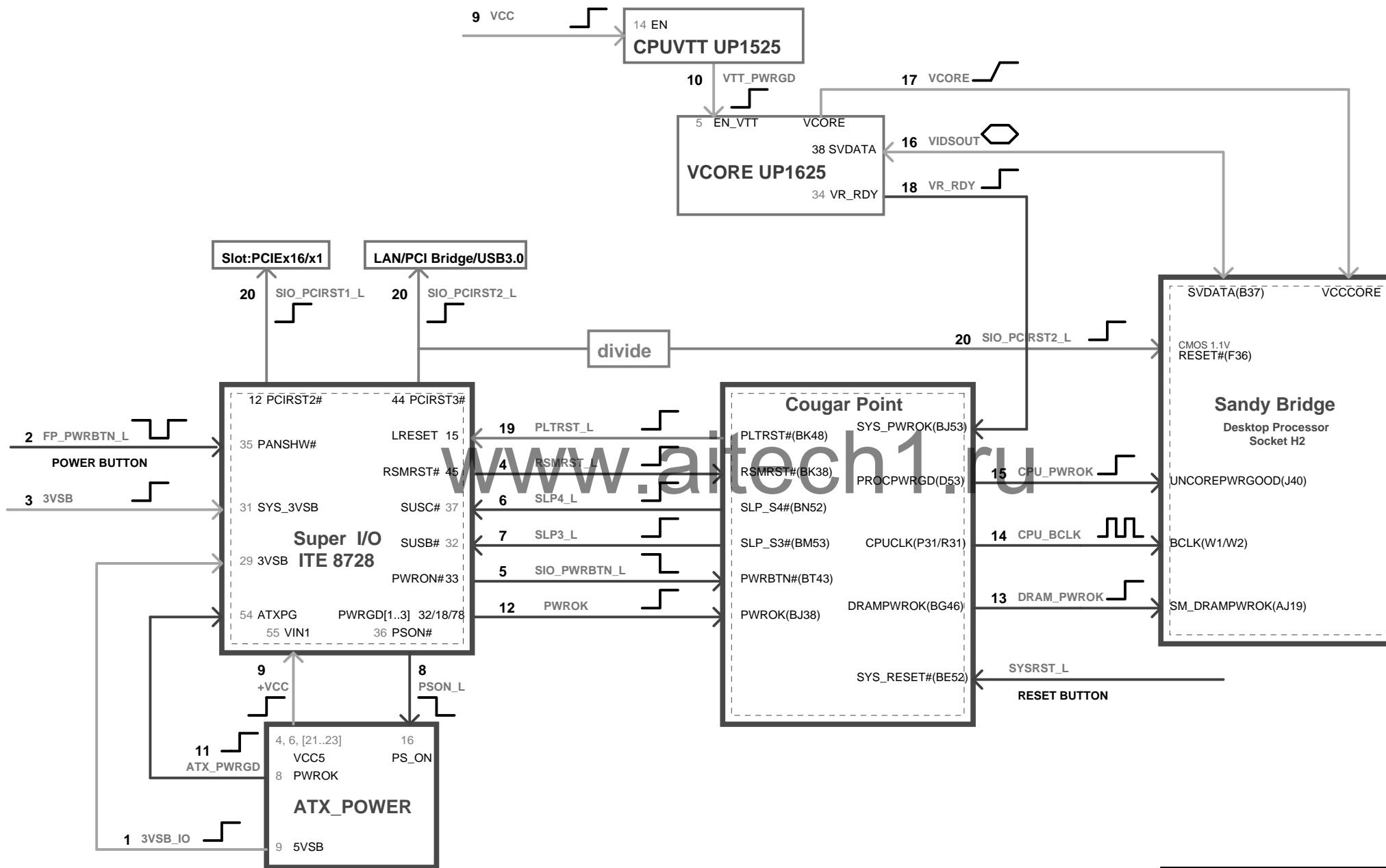
LAN_HSIP/N請接到SB的PCIE TX端

LAN_HSIP/N在SB的PCIE TX端要記得放AC coupling cap

Closed to LAN & trace need GND shielding







NOTE:

Sugar Bay Platform has two clock mode:

- 1.Integrated Clock Mode (Generate by PCH)
 - 2.Buffer Through Mode (Generate by Clock Gen.)
- If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option

